

# TFF11142HN

Low phase noise LO generator for VSAT applications

Rev. 1 — 28 March 2013

Product data sheet

## 1. General description

The TFF11142HN is a  $K_u$  band frequency generator intended for low phase noise Local Oscillator (LO) circuits for  $K_u$  band VSAT transmitters and transceivers. The specified phase noise complies with IESS-308 from Intelsat.

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

## 2. Features and benefits

- Phase noise compliant with IESS-308 (Intelsat) in combination with appropriate source
- LO generator with VCO range from 14.13 GHz to 14.42 GHz
- Input signal 55 MHz to 901 MHz
- Divider settings 16, 32, 64, 128 or 256
- Output level  $-6$  dBm; stability  $\pm 2$  dB
- Third or fourth order PLL
- Internally stabilized voltage references for loop filter

## 3. Applications

- VSAT up converters
- Local oscillator signal generation

## 4. Quick reference data

**Table 1. Quick reference data**

Operating conditions of [Table 10](#) apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		3.0	3.3	3.6	V
$I_{CC}$	supply current		-	100	130	mA
$f_{o(RF)}$	RF output frequency		14.13	-	14.42	GHz
$\varphi_{n(synth)}$	synthesizer phase noise	divider value = 64; at 100 kHz offset; reference phase noise is $-149$ dBc/Hz at 100 kHz offset	-	$-97$	$-92$	dBc/Hz
$RL_{out}$	output return loss	measured at demo board and de-embedded to footprint	-	$-10$	-	dB
$\alpha_{sup(sp)ref}$	reference spurious suppression	measured at divider value = 256	-	-	$-70$	dBc



### 5. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
TFF11142HN	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1

### 6. Marking

Table 3. Marking codes

Type number	Marking code
TFF11142HN	T142

### 7. Block diagram



Fig 1. Block diagram

8. Functional diagram

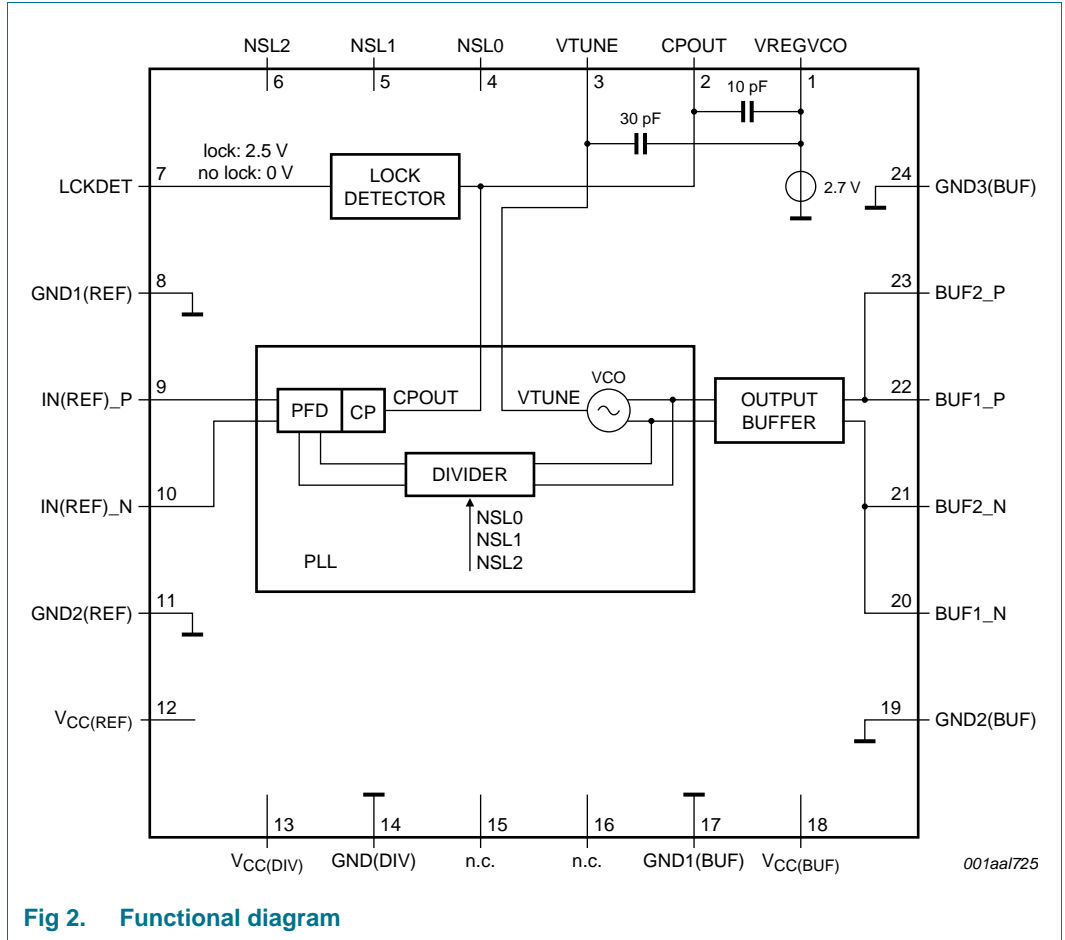


Fig 2. Functional diagram

## 9. Pinning information

### 9.1 Pinning

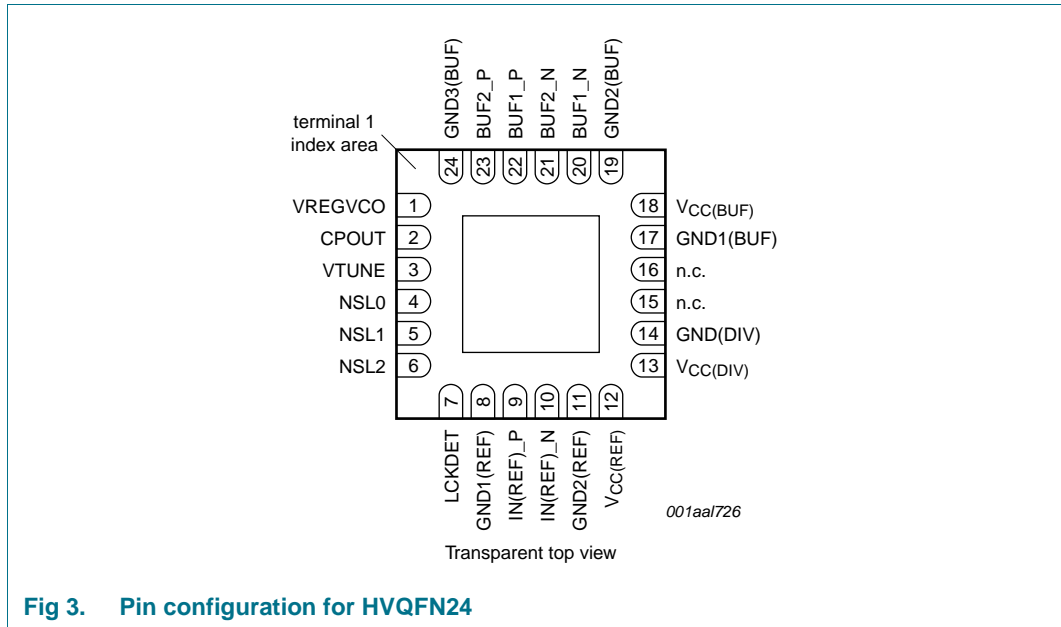


Fig 3. Pin configuration for HVQFN24

### 9.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VREGVCO	1	Regulated output voltage for VCO loop filter. Connect loop filter to this pin.
CPOUT	2	Charge pump output.
VTUNE	3	Tuning voltage for VCO.
NSL0	4	Divider setting, LSB. Leave open for "1", connect to GND for "0". See <a href="#">Table 8</a> .
NSL1	5	Divider setting. Leave open for "1", connect to GND for "0". See <a href="#">Table 8</a> .
NSL2	6	Divider setting, MSB. Leave open for "1", connect to GND for "0". See <a href="#">Table 8</a> .
LCKDET	7	Lock detect. Lock = 2.5 V; out of lock = 0 V. See <a href="#">Table 6</a> .
GND1(REF)	8	Ground for REF input. Connect this pin to the exposed diepad landing.
IN(REF)_P	9	Reference signal, non-inverting input. Couple this AC to the source.
IN(REF)_N	10	Reference signal, inverting input. Couple this AC to the source.
GND2(REF)	11	Ground for REF input. Connect this pin to the exposed diepad landing.
V <sub>CC</sub> (REF)	12	Supply of the internal regulated voltages. Decouple this pin against GND2(REF) (pin 11).
V <sub>CC</sub> (DIV)	13	Supply of the divider and PFD/CP. Decouple this pin against GND(DIV) (pin 14).
GND(DIV)	14	Ground of the divider. Connect this pin to the exposed diepad landing.
n.c.	15	not connected
n.c.	16	not connected
GND1(BUF)	17	Ground for RF output. Connect this pin to the exposed diepad landing.

**Table 4.** Pin description ...continued

Symbol	Pin	Description
V <sub>CC(BUF)</sub>	18	Supply voltage for the RF output buffer. Decouple this pin against GND2(BUF) (pin 19).
GND2(BUF)	19	Ground for RF output. Connect this pin to the exposed diepad landing.
BUF1_N	20	RF output.
BUF2_N	21	RF output.
BUF1_P	22	RF output.
BUF2_P	23	RF output.
GND3(BUF)	24	Ground for RF output. Connect this pin to the exposed diepad landing.

## 10. Functional description

The TFF11142HN consists of the following blocks:

- PLL
- Output buffer
- Lock detector
- Reference input
- Divider settings

The functionality of the blocks will be discussed below.

### 10.1 PLL

The PLL is formed by the VCO, DIVIDER (possible settings: 16, 32, 64, 128 and 256 (see [Table 8](#))) and a PFD/CP. The tune voltage is referred to the band gap regulated voltage: VREGVCO (pin 1).

The loop filter can be set to type 2 or type 3. If a type 2 filter is used, the pins CPOUT (pin 2) and VTUNE (pin 3) must be interconnected. A 10 pF capacitor is placed internally between pins CPOUT (pin 2) and VREGVCO (pin 1), and a 30 pF capacitor is placed between pins VTUNE (pin 3) and VREGVCO (pin 1). See [Figure 4](#) and [Figure 5](#). Values for the loop filter components are given in [Table 5](#).

The VCO input voltage range is between 0.1 and 0.9 V<sub>O(reg)VCO</sub>.

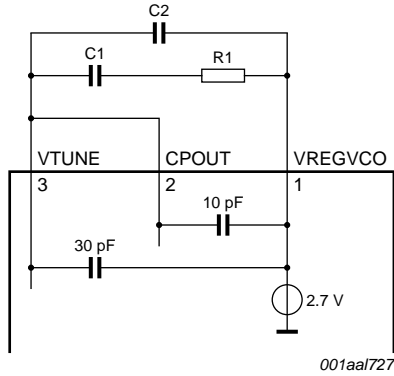


Fig 4. Type 2 loop filter

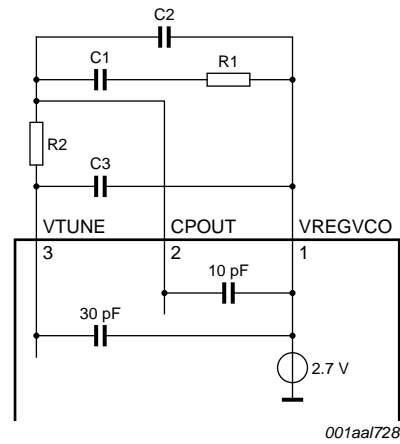


Fig 5. Type 3 loop filter

Table 5. Component values used for characterization

$f_{i(ref)}$ (MHz)	Divider value	C1 (nF)	C2 (pF)	C3 (pF)	R1 ( $\Omega$ )	R2 ( $\Omega$ )
55.195 to 56.328	256	27	82	33	470	560
110.391 to 112.656	128	18	82	33	330	560
220.781 to 225.313	64	18	120	33	270	560
441.563 to 450.625	32	33	270	33	120	560
883.125 to 901.250	16	68	560	33	68	560

### 10.2 Output buffer

The output consists of a differential pair with 50  $\Omega$  collector resistors  $R_{BUF\_P}$  and  $R_{BUF\_N}$ . If only one output is used, terminate the non used output with the same impedance as the load (see [Figure 8](#))

### 10.3 Lock detector

The lock detector is the output of a window detector. The window detector compares the output voltage over the charge pump. This voltage is identical to VTUNE when a type 2 loop filter is used (see [Figure 4](#)). In case of a type 3 loop filter this voltage is filtered by R2/C3 (see [Figure 5](#)). Due to this filtering the attack and decay time will decrease.

The lower window detector threshold voltage is 7 % of the output voltage on VREGVCO (pin 1), the upper window detector threshold voltage is 93 % of the output voltage on VREGVCO (pin 1). The hysteresis is 0.1 V. The output is 2.5 V CMOS compliant. The values are shown in [Table 6](#). The timing diagram is shown in [Figure 6](#).

At start-up the LCKDET (pin 7) will be LOW until the circuit has acquired lock.

**Table 6. Logical value and physical value for lock detect (LCKDET)**

Logical value	Physical value	Lock detect state
0	0 V	out of lock
1	2.5 V	lock

LCKDET (pin 7) has a pull-down resistor of 100 kΩ to GND1(REF) (pin 8).



### 10.4 Reference input (IN(REF)\_P, IN(REF)\_N)

The reference input is a differential pair and is internally biased. The input is high ohmic. The input signal must be AC coupled. If used in a single ended mode, the not used input must be terminated with the same impedance as the driving source.

An example of the differential source and two single ended loads are shown in [Figure 7](#). An example of a single ended application is shown in [Figure 8](#).

Note that the phase noise of the output signal is also determined by the phase noise of the reference signal. The reference frequency range is equal to the output frequency / division value. Note that the output frequency is guaranteed from 8.20 GHz to 8.60 GHz.

## 10.5 Divider settings (NSL2, NSL1, NSL0)

The divider can be set to 16, 32, 64, 128 and 256 (See [Table 8](#)). The logic levels for NSL0 (pin 4), NSL1 (pin 5) and NSL2 (pin 6) are given in [Table 7](#).

The pins have a pull-up resistor of 100 k $\Omega$  to  $V_{CC(DIV)}$  (pin 13).

The device is only guaranteed when NSL2, NSL1 and NSL0 are predefined at start-up (no change of divider value is allowed during operation).

**Table 7. Logical and physical value for divider setting (NSL2, NSL1, NSL0)**

Logical value	Physical value
0	GND
1	open or $V_{CC}$

The truth table is shown in [Table 8](#).

**Table 8. Divider setting as function of NSL2, NSL1 and NSL0**

Setting number	NSL2	NSL1	NSL0	Divider value
0	0	0	0	16
1	0	0	1	32
2	0	1	0	64
3	0	1	1	128
4	1	0	0	256
5	1	0	1	[1]
6	1	1	0	[1]
7	1	1	1	[1]

[1] Test mode, divider output will be disabled.

## 11. Limiting values

**Table 9. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage	on pin NSL0	-0.5	+5	V
		on pin NSL1	-0.5	+5	V
		on pin NSL2	-0.5	+5	V
		on pin IN(REF)_P	-0.5	+5	V
		on pin IN(REF)_N	-0.5	+5	V
		on pin $V_{CC(REF)}$	-0.5	+5	V
		on pin $V_{CC(DIV)}$	-0.5	+5	V
		on pin $V_{CC(BUF)}$	-0.5	+5	V



**Table 9. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>i</sub>	input power	on pin IN(REF)_P	-4	+10	dBm
		on pin IN(REF)_N	-4	+10	dBm
T <sub>j</sub>	junction temperature		-40	+125	°C
T <sub>stg</sub>	storage temperature		-40	+125	°C
V <sub>ESD</sub>	electrostatic discharge voltage	Human Body Model (HBM); According to JEDEC standard 22-A114E	-	2.5	kV
		Charged Device Model (CDM); According to JEDEC standard 22-C101B	-	1	kV

## 12. Recommended operating conditions

**Table 10. Operating conditions**

NSL0 (pin 4), NSL1 (pin 5) and NSL2 (pin 6) not changed during operation.

Loop filter component values as depicted in [Table 5](#) are used.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T <sub>amb</sub>	ambient temperature		-40	+25	+85	°C
Z <sub>0</sub>	characteristic impedance		-	50	-	Ω
φ <sub>n(ref)</sub>	reference phase noise	divider value = 16	[1]	-	-	-134 dBc/Hz
		divider value = 32	[1]	-	-	-143 dBc/Hz
		divider value = 64	[1]	-	-	-149 dBc/Hz
		divider value = 128	[1]	-	-	-150 dBc/Hz
		divider value = 256	[1]	-	-	-151 dBc/Hz
f <sub>i(ref)</sub>	reference input frequency	f <sub>i(ref)</sub> = f <sub>o(RF)</sub> / divider value	55	-	901	MHz
P <sub>i(ref)</sub>	reference input power		-10	-	0	dBm

[1] Required reference phase noise is set 10 dB below equivalent input phase noise.

## 13. Thermal characteristics

**Table 11. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point		25	K/W

## 14. Characteristics

**Table 12. Characteristics**

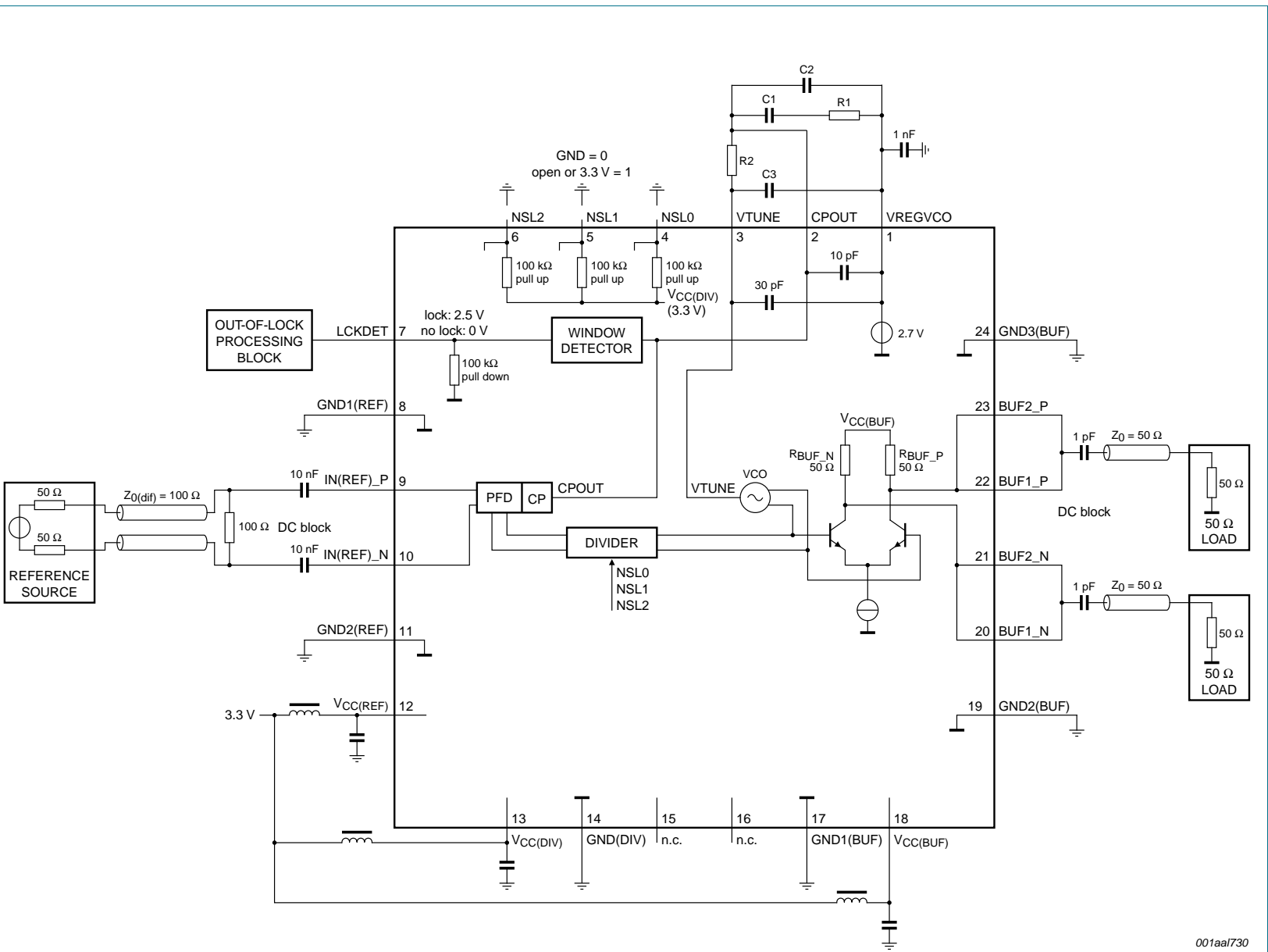
Operating conditions of [Table 10](#) apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>CC</sub>	supply voltage		3.0	3.3	3.6	V	
I <sub>CC</sub>	supply current		-	100	130	mA	
<b>PLL</b>							
f <sub>o(RF)</sub>	RF output frequency		14.13	-	14.42	GHz	
V <sub>O(reg)VCO</sub>	VCO regulator output voltage		2.5	2.7	2.9	V	
I <sub>cp</sub>	charge pump current		-	1	-	mA	
K <sub>O</sub>	VCO steepness		[1]	0.76	-	GHz/V	
φ <sub>n(VCO)</sub>	VCO phase noise	at 10 MHz offset	-	-130	-	dBc/Hz	
φ <sub>n(synth)</sub>	synthesizer phase noise	divider value = 64; at 100 kHz offset; reference phase noise is -149 dBc/Hz at 100 kHz offset	-	-97	-92	dBc/Hz	
<b>Output buffer</b>							
P <sub>o</sub>	output power	measured single ended	[2]	-8	-	-4	dBm
RL <sub>out</sub>	output return loss	measured at demo board and de-embedded to footprint	-	-10	-	dB	
α <sub>sup(sp)ref</sub>	reference spurious suppression	measured at divider value = 256	-	-	-70	dBc	
α <sub>H(LO)</sub>	LO harmonic rejection		-	-10	-	dBc	
<b>Lock detector</b>							
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = 1 mA	-	-	0.4	V	
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub> = -1 mA	2.2	-	-	V	
R <sub>pd</sub>	pull-down resistance		70	100	130	kΩ	
<b>Divider setting (NSL0, NSL1, NSL2)</b>							
R <sub>pu</sub>	pull-up resistance		70	100	130	kΩ	
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V	
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V	

[1] The typical ratio of the maximum K<sub>O</sub> in relation to the minimum K<sub>O</sub> is 1.25.

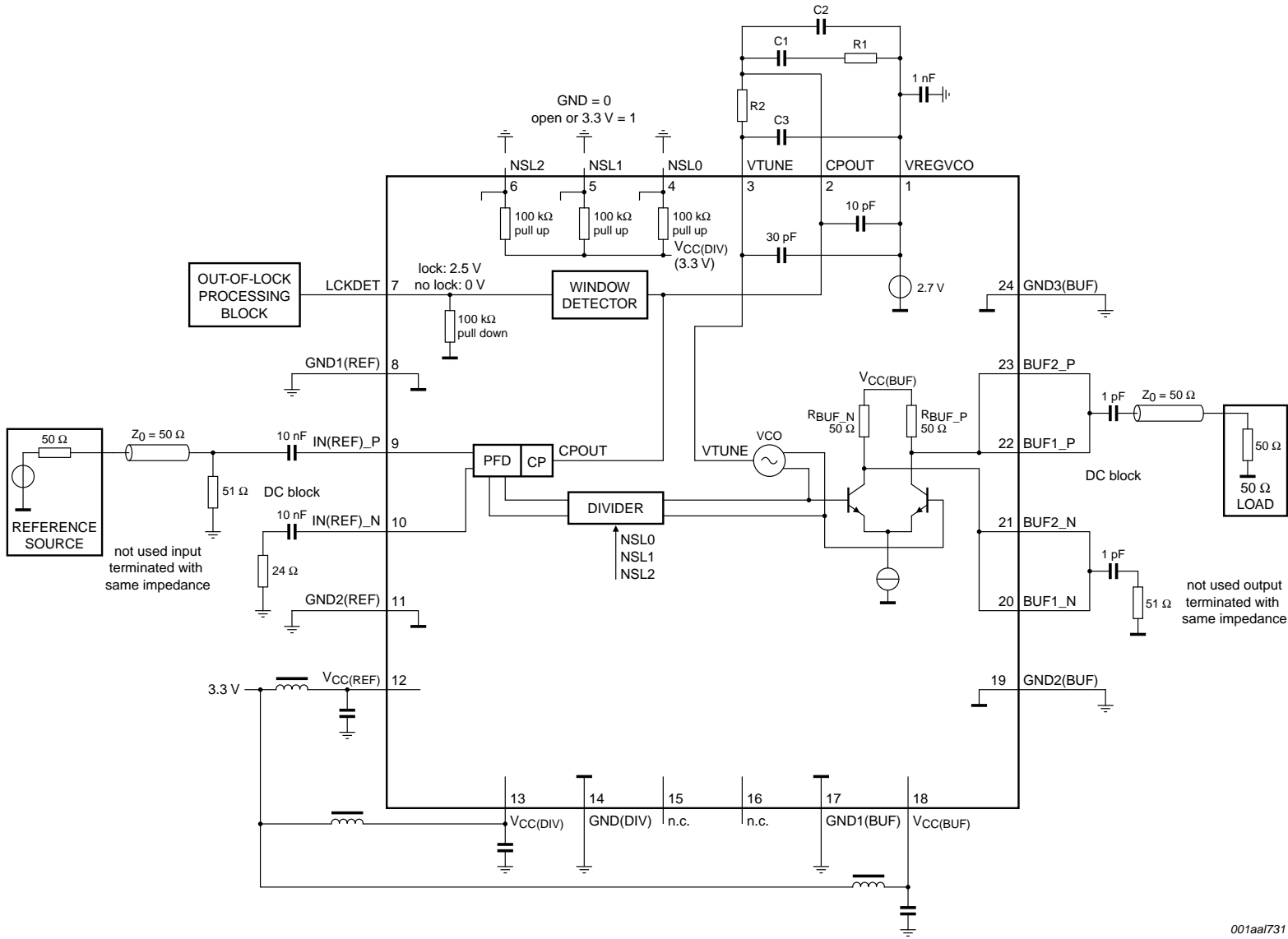
[2] Output stage is a differential pair with 50 Ω collector impedances.  
Output power is measured per output pin for the fundamental tone only.  
Output is DC coupled and is AC coupled in on-board.

### 15. Application information



001aa1730

Fig 7. Application diagram with differential source for IN(REF) and both outputs driving a load, loop filter is type 3



001aal731

Fig 8. Application diagram with single ended source for IN(REF) and single ended load, loop filter is type 3

16. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm

SOT616-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	e <sub>2</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	---	MO-220	---			01-08-08- 02-10-22

Fig 9. Package outline SOT616-1 (HVQFN24)

## 17. Abbreviations

**Table 13. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
K <sub>u</sub> band	K-under band
LSB	Least Significant Bit
MSB	Most Significant Bit
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
VCO	Voltage Controlled Oscillator
VSAT	Very Small Aperture Terminal

## 18. Revision history

**Table 14. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFF11142HN v.1	20130328	Product data sheet	-	-

## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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