GENERAL DESCRIPTION

The XRT86VL38 is an eight-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy). The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VL38 provides protection from power failures and hot swapping.

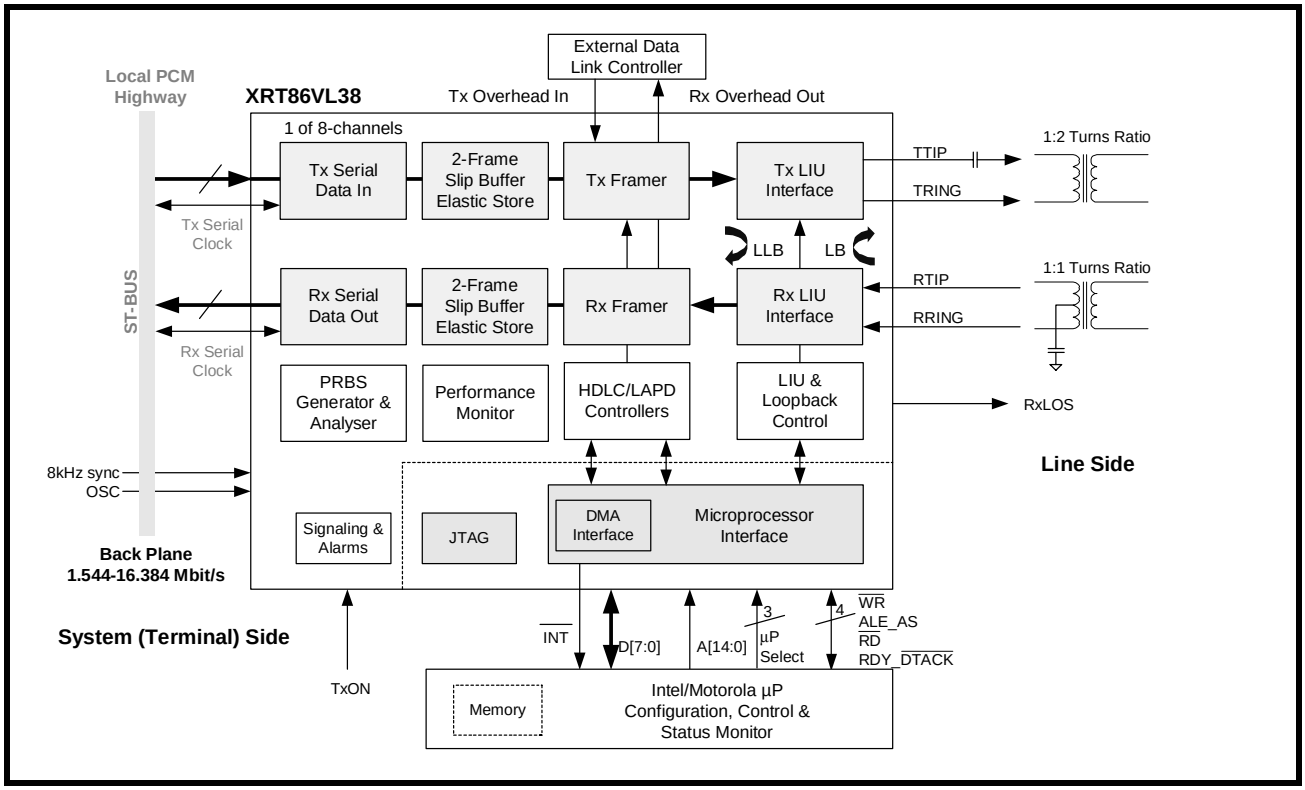
The XRT86VL38 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VL38 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VL38 8-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Eight independent, full duplex DS1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers per channel for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.

- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core Voltage
- 3.3V I/O operation with 5V tolerant inputs
- 420-pin PBGA package or 484-pin STBGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL38IB	420 Plastic Ball Grid Array	-40°C to +85°C
XRT86VL38IB484	484 Shrink Thin Ball Grid Array	-40°C to +85°C

420 BALL - PLASTIC BALL GRID ARRAY (BOTTOM VIEW, SEE PIN LIST FOR DESCRIPTION)

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O																	O	O	O	O	O	F
O	O	O	O	O																	O	O	O	O	O	G
O	O	O	O	O																	O	O	O	O	O	H
O	O	O	O	O																	O	O	O	O	O	J
O	O	O	O	O																	O	O	O	O	O	K
O	O	O	O	O																	O	O	O	O	O	L
O	O	O	O	O																	O	O	O	O	O	M
O	O	O	O	O																	O	O	O	O	O	N
O	O	O	O	O																	O	O	O	O	O	P
O	O	O	O	O																	O	O	O	O	O	R
O	O	O	O	O																	O	O	O	O	O	T
O	O	O	O	O																	O	O	O	O	O	U
O	O	O	O	O																	O	O	O	O	O	V
O	O	O	O	O																	O	O	O	O	O	W
O	O	O	O	O																	O	O	O	O	O	Y
O	O	O	O	O																	O	O	O	O	O	AA
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AB
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AC
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AD
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AE
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AF

484 BALL - SHRINK THIN BALL GRID ARRAY (BOTTOM VIEW - SEE PIN LIST FOR DESCRIPTION)

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	F
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	G
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	H
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	J
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	K
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	L
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	M
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	N
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	P
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	R
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	T
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	U
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	V
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	W
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	Y
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AA
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AB

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1.0 PIN LISTS

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
A1	DVDD18
A2	DGND
A3	AGND
A4	MCLKIN
A5	TMS
A6	RXSERCLK0
A7	TCK
A8	RXCHCLK0
A9	TXSYNC0
A10	RXCHN0_4
A11	TXSERCLK0
A12	TXCHCLK0
A13	TXCHN0_2
A14	RXCHCLK1
A15	RXCHN1_2
A16	RXLOS1
A17	TXMSYNC1
A18	TXOH1
A19	TXOHCLK1
A20	TXCHN1_3
A21	TXCHN1_4
A22	RXCHN2_0
A23	RXCASYNC2
A24	RXCHCLK2
A25	VDD
A26	RXCHN2_4
B1	VDDPLL18
B2	GNDPLL
B3	NC
B4	AVDD18
B5	E1MCLKOUT

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
B6	TDO
B7	TRST
B8	RXCRCSYNC0
B9	RXOHCLK0
B10	TXMSYNC0
B11	TEST
B12	TXCHN0_1
B13	RXSERCLK1
B14	RXSER1
B15	RXOH1
B16	RXCHN1_3
B17	VSS
B18	NC
B19	TXCHN1_2
B20	RXLOS2
B21	GPIO1_3
B22	RXCHN2_1
B23	NC
B24	TXSYNC2
B25	VSS
B26	TXCHCLK2
C1	VDDPLL18
C2	VDDPLL18
C3	GNDPLL
C4	NC
C5	ANALOG
C6	VSS
C7	RXSER0
C8	VDD
C9	RXCHN0_2
C10	RXCHN0_3
C11	RXOH0

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
C12	TXOH0
C13	VSS
C14	TXCHN0_4
C15	VDD
C16	TXSYNC1
C17	RXCHN1_4
C18	TXCHN1_0
C19	TXSERCLK1
C20	RXSERCLK2
C21	RXSER2
C22	RXCHN2_2
C23	RXCHN2_3
C24	TXMSYNC2
C25	VSS
C26	TXCHN2_2
D1	RTIP0
D2	RVDD0
D3	VDDPLL18
D4	JTAG_RING
D5	RxTSEL
D6	T1MCLKOUT
D7	TDI
D8	RXCHN0_0
D9	RXSYNC0
D10	VSS
D11	TXSER0
D12	TXCHN0_0
D13	RXCRCSYNC1
D14	RXCHN1_0
D15	RXSYNC1
D16	RXOHCLK1
D17	TXSER1

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
D18	TXCHN1_1
D19	RXSYNC2
D20	VSS
D21	RXOH2
D22	TXSERCLK2
D23	NC
D24	VDD18
D25	TXCHN2_1
D26	RXSER3
E1	RRING0
E2	RGND0
E3	GNDPLL
E4	GNDPLL
E5	NC
E6	SENSE
E7	aTEST
E8	RXLOS0
E9	RXCHN0_1
E10	RXCASYNC0
E11	TXOHCLK0
E12	VDD18
E13	TXCHN0_3
E14	RXCHN1_1
E15	RXCASYNC1
E16	NC
E17	TXCHCLK1
E18	VDD18
E19	NC
E20	RXCRCSYNC2
E21	RXOHCLK2
E22	NC
E23	TXSER2

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
E24	TXOHCLK2
E25	TXCHN2_4
E26	TXOH2
F1	RTIP1
F2	RVDD1
F3	TTIP0
F4	TVDD0
F5	JTAG_TIP
F22	TXCHN2_0
F23	TXCHN2_3
F24	VDD
F25	RXCHCLK3
F26	RXOH3
G1	RRING1
G2	RGND1
G3	TTIP1
G4	TRING0
G5	NC
G22	GPIO1_2
G23	RXSYNC3
G24	RXOHCLK3
G25	RXCRCSYNC3
G26	RXCHN3_0
H1	RTIP2
H2	RVDD2
H3	TVDD1
H4	TRING1
H5	TGND0
H22	VSS
H23	RXCASYNC3
H24	RXLOS3
H25	RXSERCLK3

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
H26	RXCHN3_1
J1	RRING2
J2	RGND2
J3	TTIP2
J4	TVDD2
J5	TGND1
J22	TXCHCLK3
J23	RXCHN3_2
J24	VDD18
J25	TXOH3
J26	RXCHN3_3
K1	RTIP3
K2	RVDD3
K3	TTIP3
K4	TRING2
K5	TGND2
K22	TXSYNC3
K23	TXOHCLK3
K24	TXSERCLK3
K25	RXCHN3_4
K26	TXSER3
L1	RRING3
L2	RGND3
L3	TVDD3
L4	TRING3
L5	TGND3
L22	TXCHN3_0
L23	VSS
L24	TXMSYNC3
L25	TXCHN3_1
L26	CS
M1	RTIP4

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
M2	RVDD4
M3	TTIP4
M4	TRING4
M5	TGND4
M22	TXCHN3_2
M23	WR
M24	TXCHN3_3
M25	DATA7
M26	TXCHN3_4
N1	RRING4
N2	RGND4
N3	TVDD4
N4	NC
N5	TGND5
N22	ADDR14
N23	ADDR13
N24	DATA6
N25	DATA5
N26	VDD
P1	RTIP5
P2	RVDD5
P3	TTIP5
P4	TRING5
P5	NC
P22	ADDR11
P23	BLAST
P24	DATA4
P25	ADDR12
P26	VSS
R1	RRING5
R2	RGND5
R3	TVDD5

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
R4	TRING6
R5	TGND6
R22	ALE
R23	ADDR9
R24	ADDR10
R25	PTYPE2
R26	INT
T1	RTIP6
T2	RVDD6
T3	TTIP6
T4	TVDD6
T5	TGND7
T22	ADDR7
T23	VDD18
T24	ADDR8
T25	DATA2
T26	DATA3
U1	RRING6
U2	RGND6
U3	TTIP7
U4	TRING7
U5	NC
U22	ADDR2
U23	ADDR3
U24	ADDR4
U25	ADDR5
U26	ADDR6
V1	RTIP7
V2	RVDD7
V3	TVDD7
V4	NC
V5	NC

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
V22	VSS
V23	DBEN
V24	RDY
V25	ADDR0
V26	ADDR1
W1	RRING7
W2	RGND7
W3	NC
W4	NC
W5	NC
W22	iADDR
W23	PTYPE0
W24	DATA1
W25	RD
W26	PTYPE1
Y1	VSS
Y2	VDD
Y3	TXON
Y4	RESET
Y5	E1OSCCLK
Y22	RXOHCLK4
Y23	ACK0
Y24	ACK1
Y25	PCLK
Y26	DATA0
AA1	VSS
AA2	8KEXTOSC
AA3	NC
AA4	NC
AA5	NC
AA22	RXOH4
AA23	VSS

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
AA24	REQ1
AA25	VDD
AA26	fADDR
AB1	LOP
AB2	TXCHCLK7
AB3	8KSYNC
AB4	TXCHN7_4
AB5	TXSERCLK7
AB6	RXSERCLK7
AB7	RXSER7
AB8	RXCHN7_0
AB9	TXSER6
AB10	TXCHN6_0
AB11	RXSYNC6
AB12	RXSERCLK6
AB13	RXCHN6_1
AB14	TXCHN5_3
AB15	TXSER5
AB16	TXOHCLK5
AB17	RXCHN5_2
AB18	GPIO0_2
AB19	VSS
AB20	VDD18
AB21	TXSER4
AB22	RXCHN4_4
AB23	VSS
AB24	RXCHCLK4
AB25	RXCRCSYNC4
AB26	REQ0
AC1	T1OSCCLK
AC2	TXOH7
AC3	TXCHN7_3

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
AC4	VDD
AC5	TXCHN7_0
AC6	RXSYNC7
AC7	RXCHN7_1
AC8	TXMSYNC6
AC9	RXCASYNC6
AC10	TXOHCLK6
AC11	VDD
AC12	RXLOS6
AC13	RXCHN6_0
AC14	TXCHN5_4
AC15	TXCHN5_0
AC16	VSS
AC17	RXCHN5_3
AC18	RXSER5
AC19	RXSERCLK5
AC20	TXCHN4_2
AC21	TXMSYNC4
AC22	VSS
AC23	RXCHN4_3
AC24	VDD18
AC25	RXSER4
AC26	RXLOS4
AD1	VDD18
AD2	TXCHN7_2
AD3	TXCHN7_1
AD4	RXLOS7
AD5	RXCRCSYNC7
AD6	VSS
AD7	VDD18
AD8	TXSYNC6
AD9	VSS

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
AD10	TXCHCLK6
AD11	GPIO0_0
AD12	RXCHN6_3
AD13	GPIO0_1
AD14	TXOH5
AD15	TXCHN5_1
AD16	TXMSYNC5
AD17	RXCHN5_4
AD18	RXCHN5_0
AD19	TXCHN4_4
AD20	GPIO0_3
AD21	TXCHN4_0
AD22	TXCHCLK4
AD23	VDD
AD24	RXCASYNC4
AD25	RXCHN4_0
AD26	RXSERCLK4
AE1	TXOHCLK7
AE2	VSS
AE3	TXSER7
AE4	TXSYNC7
AE5	RXCHN7_3
AE6	TXSERCLK6
AE7	RXOHCLK7
AE8	TXCHN6_4
AE9	TXCHN6_2
AE10	RXCRCSYNC6
AE11	RXCHCLK6
AE12	RXSER6
AE13	RXOHCLK6
AE14	RXOH6
AE15	TXCHN5_2

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
AE16	TXCHCLK5
AE17	RXOH5
AE18	VDD
AE19	RXCASYNC5
AE20	TXCHN4_3
AE21	RXCHCLK5
AE22	GPIO1_0
AE23	TXSERCLK4
AE24	GPIO1_1
AE25	RXCHN4_1
AE26	RXSYNC4
AF1	NC
AF2	TXMSYNC7
AF3	RXCHN7_4
AF4	RXCHN7_2
AF5	RXCHCLK7
AF6	RXCASYNC7
AF7	RXOH7
AF8	TXCHN6_3
AF9	TXCHN6_1
AF10	TXOH6
AF11	RXCHN6_4
AF12	RXCHN6_2
AF13	VSS
AF14	VDD18
AF15	TXSERCLK5
AF16	TXSYNC5
AF17	RXOHCLK5
AF18	RXCHN5_1
AF19	RXSYNC5
AF20	RXLOS5
AF21	RXCRCSYNC5

TABLE 1: 420 BALL LIST BY BALL NUMBER

PIN	PIN NAME
AF22	TXCHN4_1
AF23	TXOHCLK4
AF24	TXSYNC4
AF25	TXOH4
AF26	RXCHN4_2

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
A2	AVDD_LV
A4	E1MCLKOUT
A5	MCLKIN
A6	TRST
A7	RXCHN0_0
A8	RXSYNC0
A9	TXMSYNC0
A10	TXOHCLK0
A11	TXCHN0_1
A12	RXSERCLK1
A13	TXCHN0_4
A14	RXOH1
A15	RXCHN1_3
A16	TXCHCLK1
A17	TXOHCLK1
A18	RXSYNC2
A19	GPIO1_3
A20	RXCRCSYNC2
A21	RXOHCLK2
B1	VDDPLL18
B3	AGND
B5	DGND
B6	TMS
B7	RXSER0
B8	RXCRCSYNC0
B9	TXSYNC0
B10	RXCHN0_4
B11	TXCHN0_0
B12	RXCRCSYNC1
B13	RXCHN1_0
B14	RXCASYNC1

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
B15	TXMSYNC1
B16	TXOH1
B17	TXSERCLK1
B18	RXSERCLK2
B19	RXCHN2_0
B20	RXCHCLK2
B21	RXCHN2_4
B22	TXOHCLK2
C1	VDDPLL18
C2	JTAG_RING
C6	RXTSEL
C7	ATEST
C8	RXLOS0
C9	RXCHN0_1
C10	RXCASYNC0
C11	TXSERCLK0
C12	TXCHCLK0
C13	RXCHN1_1
C14	RXLOS1
C15	TXSER1
C16	TXCHN1_0
C17	TXCHN1_3
C18	RXCASYNC2
C19	RXCHN2_1
C20	TXSYNC2
C21	TXCHN2_0
C22	TXCHN2_4
D1	GNDPLL18
D2	VDDPLL18
D3	GNDPLL18
D4	ANALOG
D8	TDO

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
D9	RXSERCLK0
D10	RXCHN0_2
D11	RXOH0
D12	TXCHN0_2
D13	RXCHN1_2
D14	RXOHCLK1
D15	TXCHN1_1
D16	RXLOS2
D17	RXSER2
D18	RXOH2
D19	RXCHN2_3
D20	TXSER2
D21	TXCHN2_3
D22	RXSYNC3
E1	RVDD0
E2	GNDPLL18
E3	VDDPLL18
E4	GNDPLL18
E5	JTAG_TIP
E6	SENSE
E9	TDI
E10	RXCHCLK0
E11	RXCHN0_3
E12	TEST
E13	TXOH0
E14	RXSER1
E15	RXCHCLK1
E16	RXSYNC1
E17	TXSERCLK2
E18	TXMSYNC2
E19	TXCHCLK2
E20	TXCHN2_1

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
E21	TXOH2
E22	RXOHCLK3
F1	TRING0
F2	TVDD0
F3	TTIP_0
F4	RGND0
F5	DVDD18
F9	T1MCLKOUT
F10	TCK
F11	RXOHCLK0
F12	TXSER0
F13	TXCHN0_3
F14	TXSYNC1
F15	TXCHN1_2
F16	RXCHN1_4
F17	RXCHN2_2
F19	TXCHN2_2
F20	RXSER3
F21	RXCASYNC3
F22	RXLOS3
G1	TVDD1
G2	RTIP0
G3	RRING0
G4	TGND0
G17	TXCHN1_4
G18	GPIO1_2
G19	RXCHCLK3
G20	RXCRCSYNC3
G21	RXCHN3_1
G22	TXCHCLK3
H1	RRING1
H2	RTIP1

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
H3	RGND1
H4	TTIP1
H5	RVDD1
H18	RXOH3
H19	RXCHN3_0
H20	RXSERCLK3
H21	RXCHN3_3
H22	TXOHCLK3
J1	TRING2
J2	TVDD2
J3	TTIP2
J4	RGND2
J5	TRING1
J6	TGND1
J18	TXOH3
J19	RXCHN3_2
J20	TXSYNC3
J21	TXSERCLK3
J22	RXCHN3_4
K1	TTIP3
K2	RGND3
K3	RRING2
K4	RTIP2
K5	TGND2
K6	RVDD2
K17	TXCHN3_1
K18	TXSER3
K19	TXCHN3_0
K20	TXMSYNC3
K21	CS
K22	TXCHN3_2
L1	RRING3

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
L2	RTIP3
L3	TVDD3
L4	TRING3
L5	TGND3
L6	RVDD3
L17	TXCHN3_4
L18	ADDR13
L19	TXCHN3_3
L20	WR
L21	DATA7
L22	ADDR14
M1	RRING4
M2	RTIP4
M3	TRING4
M4	RGND4
M5	TTIP4
M6	TVDD4
M7	RVDD4
M17	BLAST
M18	ADDR11
M19	ADDR12
M20	DATA5
M21	DATA6
M22	DATA4
N1	TVDD5
N2	TTIP5
N3	RGND5
N4	RVDD5
N5	TGND4
N17	ADDR1
N18	DATA3
N19	ADDR9

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
N20	ADDR10
N21	PTYPE2
N22	INT
P1	RGND6
P2	RRING5
P3	RTIP5
P4	TGND5
P5	TRING5
P18	ADDR0
P19	ADDR7
P20	ADDR8
P21	DATA2
P22	ALE
R1	TGND6
R2	TRING6
R3	TVDD6
R4	TTIP6
R5	RVDD6
R18	iADDR
R19	RDY
R20	ADDR4
R21	ADDR5
R22	ADDR6
T1	TTIP7
T2	RTIP6
T3	RRING6
T4	RGND7
T5	RVDD7
T18	fADDR
T19	DATA0
T20	PTYPE1
T21	ADDR2

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
T22	ADDR3
U1	TVDD7
U2	TRING7
U3	RRING7
U4	RTIP7
U5	8KEXTOSC
U7	TXCHN7_4
U8	RXLOS7
U9	TXSERCLK6
U10	TXSER6
U11	TXOH6
U12	RXOH6
U13	TXOHCLK5
U14	RXCHN5_0
U15	TXCHN4_1
U16	GPIO0_3
U17	TXMSYNC4
U18	RXCHCLK4
U19	REQ0
U20	DATA1
U21	RD
U22	DBEN
V1	TGND7
V2	LOP
V3	T1OSCCLK
V4	E1OSCCLK
V5	TXCHCLK7
V6	TXOHCLK7
V7	TXSERCLK7
V8	TXCHN7_1
V9	RXCRCSYNC7
V10	RXOH7

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
V11	TXCHCLK6
V12	RXCHN6_1
V13	TXSYNC5
V14	RXCHN5_3
V15	GPIO0_2
V16	RXSERCLK5
V17	RXCASYNC4
V18	RXOH4
V19	RXOHCLK4
V20	PTYPE0
V21	ACK1
V22	PCLK
W1	TXON
W2	8KSYNC
W3	TXSER7
W4	TXCHN7_0
W5	TXMSYNC7
W6	RXSERCLK7
W7	RXCHN7_4
W8	RXCHN7_1
W9	TXCHN6_4
W10	RXCASYNC7
W11	TXCHN6_0
W12	RXSERCLK6
W13	TXCHN5_2
W14	RXCHN5_4
W15	RXLOS5
W16	TXCHN4_0
W17	TXOH4
W18	RXCHN4_2
W19	RXSER4
W20	RXSERCLK4

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
W21	RXLOS4
W22	ACK0
Y1	RESET
Y2	TXCHN7_3
Y3	RXSYNC7
Y4	RXCHN7_2
Y5	RXCHCLK7
Y6	RXOHCLK7
Y7	RXCHN7_0
Y8	RXCASYNC6
Y9	RXCRCSYNC6
Y10	RXLOS6
Y11	GPIO0_1
Y12	TXCHN5_3
Y13	TXCHCLK5
Y14	RXOH5
Y15	RXSYNC5
Y16	TXCHN4_2
Y17	TXSYNC4
Y18	TXSERCLK4
Y19	RXCHN4_4
Y20	RXSYNC4
Y21	RXCRCSYNC4
Y22	REQ1
AA1	TXOH7
AA2	TXSYNC7
AA3	RXCHN7_3
AA4	TXSYNC6
AA5	TXCHN6_2
AA6	RXSYNC6
AA7	TXOHCLK6
AA8	RXCHCLK6

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
AA9	RXSER6
AA10	RXCHN6_0
AA11	TXOH5
AA12	TXSERCLK5
AA13	TXSER5
AA14	RXOHCLK5
AA15	RXSER5
AA16	TXCHN4_4
AA17	RXCRCSYNC5
AA18	GPIO1_0
AA19	TXCHCLK4
AA20	GPIO1_1
AA21	RXCHN4_1
AA22	RXCHN4_0
AB1	TXCHN7_2
AB2	RXSER7
AB3	TXMSYNC6
AB4	TXCHN6_3
AB5	TXCHN6_1
AB6	GPIO0_0
AB7	RXCHN6_4
AB8	RXCHN6_3
AB9	RXCHN6_2
AB10	RXOHCLK6
AB11	TXCHN5_4
AB12	TXCHN5_1
AB13	TXCHN5_0
AB14	TXMSYNC5
AB15	RXCHN5_2
AB16	RXCHN5_1
AB17	RXCASYNC5
AB18	TXCHN4_3

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
AB19	RXCHCLK5
AB20	TXOHCLK4
AB21	TXSER4
AB22	RXCHN4_3
POWER PINS	
Pin	Pin Name
G11	VDD18
G14	VDD18
G16	VDD18
J17	VDD18
P17	VDD18
T8	VDD18
T10	VDD18
T12	VDD18
T14	VDD18
T17	VDD18
G10	VDD
G12	VDD
G15	VDD
H17	VDD
L16	VDD
R17	VDD
T7	VDD
T9	VDD
T11	VDD
T13	VDD
T15	VDD
GROUND PINS	
Pin	Pin Name
F6	VSS
G6	VSS
G7	VSS

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
G8	VSS
G9	VSS
G13	VSS
H6	VSS
H7	VSS
H16	VSS
J7	VSS
J16	VSS
K7	VSS
K16	VSS
L7	VSS
M16	VSS
N6	VSS
N7	VSS
N16	VSS
P6	VSS
P7	VSS
P16	VSS
R6	VSS
R7	VSS
R16	VSS
T6	VSS
T16	VSS
U6	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS
H12	VSS
H13	VSS
H14	VSS
H15	VSS

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VSS
J14	VSS
J15	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VSS
K14	VSS
K15	VSS
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L12	VSS
L13	VSS
L14	VSS
L15	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VSS
M14	VSS
M15	VSS

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
P8	VSS
P9	VSS
P10	VSS
P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
R8	VSS
R9	VSS
R10	VSS
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
NO CONNECT PINS	
A1	NC
A3	NC
A22	NC
B2	NC
C3	NC
C4	NC
C5	NC

TABLE 2: 484 BALL LIST BY BALL NUMBER

PIN	PIN NAME
D5	NC
D6	NC
D7	NC
E7	NC
E8	NC
F7	NC
F8	NC
G5	NC
B4	NC
F18	NC

2.0 PIN DESCRIPTIONS

There are six types of pins defined throughout this pin description and the corresponding symbol is presented in table below. The per-channel pin is indicated by the channel number or the letter 'n' which is appended at the end of the signal name, for example, TxSERn, where "n" indicates channels 0 to 7. All output pins are "tri-stated" upon hardware RESET.

SYMBOL	PIN TYPE
I	Input
O	Output
I/O	Bidirectional
GND	Ground
PWR	Power
NC	No Connect

The structure of the pin description is divided into fourteen groups, as presented in the table below

TABLE 3: PIN DESCRIPTION STRUCTURE

SECTION	PAGE NUMBER
Transmit System Side Interface	page 15
Transmit Overhead Interface	page 23
Receive Overhead Interface	page 25
Receive System Side Interface	page 26
Receive Line Interface	page 34
Transmit Line Interface	page 35
Timing Interface	page 36
GPIO Interface	page 38
JTAG Interface	page 39
Microprocessor Interface	page 40
Power Pins (3.3V)	page 49
Power Pins (1.8V)	page 50
Ground Pins	page 51
No Connect Pins	page 53

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSER0/ TxPOS0 TxSER1/ TxPOS1 TxSER2/ TxPOS2 TxSER3/ TxPOS3 TxSER4/ TxPOS4 TxSER5/ TxPOS5 TxSER6/ TxPOS6 TxSER7/ TxPOS7	D11 D17 E23 K26 AB21 AB15 AB9 AE3	F12 C15 D20 K18 AB21 AA13 U10 W3	I	-	**Transmit Serial Data Input (TxSERn)/Transmit Positive Digital Input (TxPOSn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - TxSERn** These pins function as the transmit serial data input on the system side interface, which are latched on the rising edge of the TxSERCLKn pin. Any payload data applied to this pin will be inserted into an outbound DS1/E1 frame and output to the line. In DS1 mode, the framing alignment bits, facility data link bits, CRC-6 bits, and signaling information can also be inserted from this input pin if configured appropriately. In E1 mode, all data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31 must be applied to this input pin. Data intended for Time Slots 0 and 16 can also be applied to this input pin If configured accordingly. **DS1 or E1 High-Speed Multiplexed Mode* - TxSERn** In this mode, these pins are used as the high-speed multiplexed data input pin on the system side. High-speed multiplexed data of channels 0-3 must be applied to TxSER0 and high-speed multiplexed data of channels 4-7 must be applied to TxSER4 in a byte or bit-interleaved way. The framer latches in the multiplexed data on TxSER0 and TxSER4 using TxMSYNC/TxINCLK and demultiplexes this data into 4 serial streams. The LIU block will then output the data to the line interface using TxSERCLKn. **DS1 or E1 Framer Bypass Mode - TxPOSn** In this mode, TxSERn is used for the positive digital input pin (TxPOSn) to the LIU. ***NOTE:*** 1. **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* 2. *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* 3. *These 8 pins are internally pulled "High" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSERCLK0/ TxLINECLK0 TxSERCLK1/ TxLINECLK1 TxSERCLK2/ TxLINECLK2 TxSERCLK3/ TxLINECLK3 TxSERCLK4/ TxLINECLK4 TxSERCLK5/ TxLINECLK5 TxSERCLK6/ TxLINECLK6 TxSERCLK7/ TxLINECLK7	A11 C19 D22 K24 AE23 AF15 AE6 AB5	C11 B17 E17 J21 Y18 AA12 U9 V7	I/O	12	**Transmit Serial Clock (TxSERCLKn)/Transmit Line Clock (TxSERCLKn):** The exact function of these pins depends on the mode of operation selected, as described below. **In Base-Rate Mode (1.544MHz/2.048MHz) - TxSERCLKn:** This clock signal is used by the transmit serial interface to latch the contents on the TxSERn pins into the T1/E1 framer on the rising edge of the TxSERCLKn. These pins can be configured as input or output as described below. **When TxSERCLKn is configured as Input:** These pins will be inputs if the TxSERCLK is chosen as the timing source for the transmit framer. Users must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode. **When TxSERCLKn is configured as Output:** These pins will be outputs if either the recovered line clock or the MCLK PLL is chosen as the timing source for the T1/E1 transmit framer. The transmit framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode. **DS1/E1 High-Speed Backplane Modes* - TxSERCLKn as INPUT ONLY** In this mode, TxSERCLK is an optional clock signal input which is used as the timing source for the transmit line interface, and is only required if TxSERCLK is chosen as the timing source for the transmit framer. If TxSERCLK is chosen as the timing source, system equipment should provide 1.544MHz (For T1 mode) or 2.048MHz (For E1 mode) to the TxSERCLKn pins on each channel. TxSERCLK is not required if either the recovered clock or MCLK PLL is chosen as the timing source of the device. High speed or multiplexed data is latched into the device using the TxMSYNC/TxINCLK high-speed clock signal. **DS1 or E1 Framer Bypass Mode - TxLINECLKn** In this mode, TxSERCLKn is used as the transmit line clock (TxLINECLK) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSYNC0/ TxNEG0 TxSYNC1/ TxNEG1 TxSYNC2/ TxNEG2 TxSYNC3/ TxNEG3 TxSYNC4/ TxNEG4 TxSYNC5/ TxNEG5 TxSYNC6/ TxNEG6 TxSYNC7/ TxNEG7	A9 C16 B24 K22 AF24 AF16 AD8 AE4	B9 F14 C20 J20 Y17 V13 AA4 AA2	I/O	12	**Transmit Single Frame Sync Pulse (TxSYNCn) / Transmit Negative Digital Input (TxNEGn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxSYNCn:** These TxSYNCn pins are used to indicate the single frame boundary within an outbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, TxSYNCn can be configured as either input or output as described below. **When TxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/ E1 frame. It is imperative that the TxSYNC input signal be synchronized with the TxSERCLK input signal. **When TxSYNCn is configured as an Output:** The transmit T1/E1 framer will output a signal which pulses "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - TxSYNCn as INPUT ONLY:** In this mode, TxSYNCn must be an input regardless of the clock source that is chosen to be the timing source for the transmit framer. In 2.048MVIP/4.096/8.192MHz high-speed modes, TxSYNCn pins must be pulsed 'High' for one period of TxSERCLK during the first bit of the outbound T1/E1 frame. In HMVIP mode, TxSYNC0 and TxSYNC4 must be pulsed 'High' for 4 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, TxSYNC0 and TxSYNC4 must be pulsed 'High' for 2 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - TxNEGn** In this mode, TxSYNCn is used as the negative digital input pin (TxNEG) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxMSYNC0/ TxINCLK0 TxMSYNC1/ TxINCLK1 TxMSYNC2/ TxINCLK2 TxMSYNC3/ TxINCLK3 TxMSYNC4/ TxINCLK4 TxMSYNC5/ TxINCLK5 TxMSYNC6/ TxINCLK6 TxMSYNC7/ TxINCLK7	B10 A17 C24 L24 AC21 AD16 AC8 AF2	A9 B15 E18 K20 U17 AB14 AB3 W5	I/O	12	**Multiframe Sync Pulse (TxMSYNCn) / Transmit Input Clock (TxINCLKn)** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxMSYNCn** In this mode, these pins are used to indicate the multi-frame boundary within an outbound DS1/E1 frame. In DS1 ESF mode, TxMSYNCn repeats every 3ms. In DS1 SF mode, TxMSYNCn repeats every 1.5ms. In E1 mode, TxMSYNCn repeats every 2ms. If TxMSYNCn is configured as an input, TxMSYNCn must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 multi-frame. It is imperative that the TxMSYNC input signal be synchronized with the TxSERCLK input signal. If TxMSYNCn is configured as an output, the transmit section of the T1/E1 framer will output and pulse TxMSYNC "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - (TxINCLKn as INPUT ONLY)** In this mode, this pin must be used as the high-speed input clock pin (TxINCLKn) for the backplane interface to latch in high-speed or multiplexed data on the TxSERn pin. The frequency of TxINCLK is presented in the table below.

OPERATION MODE	FREQUENCY OF TXINCLK(MHZ)
2.048MVIP non-multiplexed	2.048
4.096MHz non-multiplexed	4.096
8.192MHz non-multiplexed	8.192
12.352MHz Bit-multiplexed (DS1 ONLY)	12.352
16.384MHz Bit-multiplexed	16.384
16.384 HMVIP Byte-multiplexed	16.384
16.384 H.100 Byte-multiplexed	16.384

NOTES:

1. **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.*
2. *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*
3. *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHCLK0 TxCHCLK1 TxCHCLK2 TxCHCLK3 TxCHCLK4 TxCHCLK5 TxCHCLK6 TxCHCLK7	A12 E17 B26 J22 AD22 AE16 AD10 AB2	C12 A16 E19 G22 AA19 Y13 V11 V5	O	8	**Transmit Channel Clock Output Signal (TxCHCLKn):** The exact function of this pin depends on whether or not the transmit framer enables the transmit fractional/signaling interface to input fractional data, as described below. **If transmit fractional/signaling interface is disabled:** This pin indicates the boundary of each time slot of an outbound DS1/E1 frame. In T1 mode, each of these output pins is a 192kHz clock which pulses "High" during the LSB of each 24 time slots. In E1 mode, each of these output pins is a 256kHz clock which pulses "High" during the LSB of each 32 time slots. The Terminal Equipment can use this clock signal to sample the TxCHN0 through TxCHN4 time slot identifier pins to determine which time slot is being processed. **If transmit fractional/signaling interface is enabled:** TxCHCLKn is the fractional interface clock which either outputs a clock signal for the time slot that has been configured to input fractional data, or outputs an enable signal for the fractional time slot so that fractional data can be clocked into the device using the TxSERCLK pin. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN0_0/ TxSIG0 TxCHN1_0/ TxSIG1 TxCHN2_0/ TxSIG2 TxCHN3_0/ TxSIG3 TxCHN4_0/ TxSIG4 TxCHN5_0/ TxSIG5 TxCHN6_0/ TxSIG6 TxCHN7_0/ TxSIG7	D12 C18 F22 L22 AD21 AC15 AB10 AC5	B11 C16 C21 K19 W16 AB13 W11 W4	I/O	8	**Transmit Time Slot Octet Identifier Output 0 (TxCHNn_0) / Transmit Serial Signaling Input (TxSIGn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_0:** These output pins (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates the Least Significant Bit (LSB) of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxSIGn:** These pins can be used to input robbed-bit signaling data to be inserted within an outbound DS1 frame or to input Channel Associated Signaling (CAS) data within an outbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel must be provided on bit 4,5,6,7 of each time slot on the TxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel must be provided on bit 4, 5 of each time slot on the TxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel must be provided on bit 4 of each time slot on the TxSIG pin. **E1 Mode:** Signaling data in E1 mode can be provided on the TxSIGn pins on a time-slot-basis as in T1 mode, or it can be provided on time slot 16 only via the TxSIGn input pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN0_1/ TxFrTD0 TxCHN1_1/ TxFrTD1 TxCHN2_1/ TxFrTD2 TxCHN3_1/ TxFrTD3 TxCHN4_1/ TxFrTD4 TxCHN5_1/ TxFrTD5 TxCHN6_1/ TxFrTD6 TxCHN7_1/ TxFrTD7	B12 D18 D25 L25 AF22 AD15 AF9 AD3	A11 D15 E20 K17 U15 AB12 AB5 V8	I/O	8	**Transmit Time Slot Octet Identifier Output 1 (TxCHNn_1) / Transmit Serial Fractional Input (TxFrTDn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_1** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates Bit 1 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxFrTDn** These pins are used as the fractional data input pins to input fractional DS1/E1 payload data which will be inserted within an outbound DS1/E1 frame. In this mode, terminal equipment can use either TxCHCLK or TxSERCLK to clock in fractional DS1/E1 payload data depending on the framer configuration. ***NOTES:*** *1. Transmit fractional/Signaling interface can be enabled by programming to bit 4 - TxFr1544/ TxFr2048 bit from register 0xn120 to '1'.* *2. These 8 pins are internally pulled "Low" for each channel.*
TxCHN0_2/ Tx32MHz0 TxCHN1_2/ Tx32MHz1 TxCHN2_2/ Tx32MHz2 TxCHN3_2/ Tx32MHz3 TxCHN4_2/ Tx32MHz4 TxCHN5_2/ Tx32MHz5 TxCHN6_2/ Tx32MHz6 TxCHN7_2/ Tx32MHz7	A13 B19 C26 M22 AC20 AE15 AE9 AD2	D12 F15 F19 K22 Y16 W13 AA5 AB1	O	8	**Transmit Time Slot Octet Identifier Output 2 (TxCHNn_2) / Transmit 32.678MHz Clock Output (Tx32MHZ):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_2** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates Bit 2 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - Tx32MHz** These pins are used to output a 32.678MHz clock reference which is derived from the MCLKIN input pin. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxCHN0_3/ TxOHSYNC0 TxCHN1_3/ TxOHSYNC1 TxCHN2_3/ TxOHSYNC2 TxCHN3_3/ TxOHSYNC3 TxCHN4_3/ TxOHSYNC4 TxCHN5_3/ TxOHSYNC5 TxCHN6_3/ TxOHSYNC6 TxCHN7_3/ TxOHSYNC7	E13 A20 F23 M24 AE20 AB14 AF8 AC3	F13 C17 D21 L19 AB18 Y12 AB4 Y2	O	8	**Transmit Time Slot Octet Identifier Output 3 (TxCHNn_3) / Transmit Overhead Synchronization Pulse (TxOHSYNCn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled - TxCHNn_3** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates Bit 3 of the time slot channel being processed. **If transmit fractional/signaling interface is enabled - TxOHSYNCn** These pins are used to output an Overhead Synchronization Pulse which indicates the first bit of each multi-frame. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.*
TxCHN0_4 TxCHN1_4 TxCHN2_4 TxCHN3_4 TxCHN4_4 TxCHN5_4 TxCHN6_4 TxCHN7_4	C14 A21 E25 M26 AD19 AC14 AE8 AB4	A13 G17 C22 L17 AA16 AB11 W9 U7	O	8	**Transmit Time Slot Octet Identifier Output-Bit 4 (TxCHNn_4):** These output signals (TxCHNn_4 through TxCHNn_0) reflect the five-bit binary value of the current time slot being processed by the transmit serial interface. Terminal Equipment can use the TxCHCLK to sample the five output pins of each channel in order to identify the time slot being processed. This pin indicates the Most Significant Bit (MSB) of the time slot channel being processed.

TRANSMIT OVERHEAD INTERFACE

SIGNAL NAME	420 PKG BALL #	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxOH0 TxOH1 TxOH2 TxOH3 TxOH4 TxOH5 TxOH6 TxOH7	C12 A18 E26 J25 AF25 AD14 AF10 AC2	E13 B16 E21 J18 W17 AA11 U11 AA1	I	-	**Transmit Overhead Input (TxOHn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1 Mode** These pins operate as the source of Datalink bits which will be inserted into the Datalink bits within an outbound DS1 frame if the framer is configured accordingly. Datalink Equipment can provide data to this input pin using the TxOHCLKn clock at either 2kHz or 4kHz depending on the transmit datalink bandwidth selected. ***NOTE:*** *This input pin will be disabled if the framer is using the Transmit HDLC Controller, or the TxSER input as the source for the Data Link Bits.* **E1 Mode** These pins operate as the source of Datalink bits or Signaling bits depending on the framer configuration, as described below. **Sourcing Datalink bits from TxOHn:** The E1 transmit framer will output a clock edge on TxOHCLKn for each Sa bit that has been configured to carry datalink information. Terminal equipment can then use TxOHCLKn to provide datalink bits on TxOHn to be inserted into the Sa bits within an outbound E1 frame. **Sourcing Signaling bits from TxOHn:** Users must provide signaling data on TxOHn pins on time slot 16 only. Signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxOHn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxOHn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxOHn pin during time slot 16 of frame 0. ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT OVERHEAD INTERFACE

SIGNAL NAME	420 PKG BALL #	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxOHCLK0 TxOHCLK1 TxOHCLK2 TxOHCLK3 TxOHCLK4 TxOHCLK5 TxOHCLK6 TxOHCLK7	E11 A19 E24 K23 AF23 AB16 AC10 AE1	A10 A17 B22 H22 AB20 U13 AA7 V6	O	8	**Transmit OH Serial Clock Output Signal(TxOHCLKn)** This pin functions as an overhead output clock signal for the transmit overhead interface, and its function is explained below. **DS1 Mode** If the TxOH pins have been configured to be the source for Datalink bits, the DS1 transmit framer will provide a clock edge for each Data Link Bit. In DS1 ESF mode, the TxOHCLK can either be a 2kHz or 4kHz output signal depending on the selection of Data Link Bandwidth (Register 0xn10A). Data Link Equipment can provide data to the TxOHn pin on the rising edge of TxOHCLK. The framer latches the data on the falling edge of this clock signal. **E1 Mode** If the TxOH pins have been configured to be the source for Data Link bits, the E1 transmit framer will provide a clock edge for each National Bit (Sa bits) that has been configured to carry data link information. (Register 0xn10A)

RECEIVE OVERHEAD INTERFACE

SIGNAL NAME	420 PKG BALL #	484 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
RxOH0 RxOH1 RxOH2 RxOH3 RxOH4 RxOH5 RxOH6 RxOH7	C11 B15 D21 F26 AA22 AE17 AE14 AF7	D11 A14 D18 H18 V18 Y14 U12 V10	O	8	**Receive Overhead Output (RxOHn):** These pins function as the Receive Overhead output, or Receive Signaling Output depending on the receive framer configuration, as described below. **DS1 Mode** If the RxOH pins have been configured as the destination for the Data Link bits within an inbound DS1 frame, datalink bits will be output to the RxOHn pins at either 2kHz or 4kHz depending on the Receive datalink bandwidth selected. (Register 0xn10C). If configured appropriately, signaling information in the receive signaling array registers (Registers 0xn500-0xn51F) can also be output to the RxOHn output pins. **E1 Mode** These output pins will always output the contents of the National Bits (Sa4 through Sa8) if these Sa bits have been configured to carry Data Link information (Register 0xn10C). The Receive Overhead Output Interface will provide a clock edge on RxOHCLKn for each Sa bit carrying Data Link information. If configured appropriately, signaling information in the receive signaling array registers (Registers 0xn500-0xn51F) can also be output to the RxOHn output pins.
RxOHCLK0 RxOHCLK1 RxOHCLK2 RxOHCLK3 RxOHCLK4 RxOHCLK5 RxOHCLK6 RxOHCLK7	B9 D16 E21 G24 Y22 AF17 AE13 AE7	F11 D14 A21 E22 V19 AA14 AB10 Y6	O	8	**Receive Overhead Clock Output (RxOHCLKn):** This pin functions as an overhead output clock signal for the receive overhead interface, and its function is explained below. **DS1 Mode** If the RxOH pins have been configured to be the destination for Datalink bits, the DS1 transmit framer will output a clock edge for each Data Link Bit. In DS1 ESF mode, the RxOHCLK can either be a 2kHz or 4kHz output signal depending on the selection of Data Link Bandwidth (Register 0xn10C). Data Link Equipment can clock out datalink bits on the RxOHn pin using this clock signal. **E1 Mode** The E1 receive framer provides a clock edge for each National Bit (Sa bits) that is configured to carry data link information. Data Link Equipment can clock out datalink bits on the RxOHn pin using this clock signal.

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSYNC0/ RxNEG0 RxSYNC1/ RxNEG1 RxSYNC2/ RxNEG2 RxSYNC3/ RxNEG3 RxSYNC4/ RxNEG4 RxSYNC5/ RxNEG5 RxSYNC6/ RxNEG6 RxSYNC7/ RxNEG7	D9 D15 D19 G23 AE26 AF19 AB11 AC6	A8 E16 A18 D22 Y20 Y15 AA6 Y3	I/O	12	**Receive Single Frame Sync Pulse (RxSYNCn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - RxSYNCn:** These RxSYNCn pins are used to indicate the single frame boundary within an inbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, RxSYNCn can be configured as either input or output depending on the slip buffer configuration as described below. **When RxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of RxSERCLK and repeats every 125µS. The receive serial Interface will output the first bit of an inbound DS1/E1 frame during the provided RxSYNC pulse. ***NOTE:*** *It is imperative that the RxSYNC input signal be synchronized with the RxSERCLK input signal.* **When RxSYNCn is configured as an Output:** The receive T1/E1 framer will output a signal which pulses "High" for one period of RxSERCLK during the first bit of an inbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - RxSYNCn as INPUT ONLY:** In this mode, RxSYNCn must be an input regardless of the slip buffer configuration. In 2.048MVIP/4.096/ 8.192MHz high-speed modes, RxSYNCn pins must be pulsed 'High' for one period of RxSERCLK during the first bit of the inbound T1/E1 frame. In HMVIP mode, RxSYNCn must be pulsed 'High' for 4 clock cycles of the RxSERCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, RxSYNCn must be pulsed 'High' for 2 clock cycles of the RxSERCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - RxNEGn** In this mode, RxSYNCn is used as the Receive negative digital output pin (RxNEG) from the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/ E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCRCSYNC0 RxCRCSYNC1 RxCRCSYNC2 RxCRCSYNC3 RxCRCSYNC4 RxCRCSYNC5 RxCRCSYNC6 RxCRCSYNC7	B8 D13 E20 G25 AB25 AF21 AE10 AD5	B8 B12 A20 G20 Y21 AA17 Y9 V9	O	12	**Receive Multiframe Sync Pulse (RxCRCSYNCn):** The RxCRCSYNCn pins are used to indicate the receive multi-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an inbound DS1/E1 Multi-frame is being output on the RxCRCSYNCn pin. • In DS1 ESF mode, RxCRCSYNCn repeats every 3ms • In DS1 SF mode, RxCRCSYNCn repeats every 1.5ms • In E1 mode, RxCRCSYNCn repeats every 2ms.
RxCASYNC0 RxCASYNC1 RxCASYNC2 RxCASYNC3 RxCASYNC4 RxCASYNC5 RxCASYNC6 RxCASYNC7	E10 E15 A23 H23 AD24 AE19 AC9 AF6	C10 B14 C18 F21 V17 AB17 Y8 W10	O	12	**Receive CAS Multiframe Sync Pulse (RxCASYNCn):** **- E1 Mode Only** The RxCASYNCn pins are used to indicate the E1 CAS Multif-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an E1 CAS Multi-frame is being output on the RxCASYNCn pin.

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSERCLK0/ RxLINECLK0 RxSERCLK1/ RxLINECLK1 RxSERCLK2/ RxLINECLK2 RxSERCLK3/ RxLINECLK3 RxSERCLK4/ RxLINECLK4 RxSERCLK5/ RxLINECLK5 RxSERCLK6/ RxLINECLK6 RxSERCLK7/ RxLINECLK7	A6 B13 C20 H25 AD26 AC19 AB12 AB6	D9 A12 B18 H20 W20 V16 W12 W6	I/O	12	**Receive Serial Clock Signal (RxSERCLKn) / Receive Line Clock (RxLINECLKn):** The exact function of these pins depends on the mode of operation selected, as described below. **In Base-Rate Mode (1.544MHz/2.048MHz) - RxSERCLKn:** These pins are used as the receive serial clock on the system side interface which can be configured as either input or output. The receive serial interface outputs data on RxSERn on the rising edge of RxSERCLKn. **When RxSERCLKn is configured as Input:** These pins will be inputs if the slip buffer on the Receive path is enabled. System side equipment must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode. **When RxSERCLKn is configured as Output:** These pins will be outputs if slip buffer is bypassed. The receive framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode. **DS1/E1 High-Speed Backplane Modes* - (RxSERCLK as INPUT ONLY)** In this mode, this pin must be used as the high-speed input clock for the backplane interface to output high-speed or multiplexed data on the RxSERn pin. The frequency of RxSERCLK is presented in the table below.

OPERATION MODE	FREQUENCY OF RXSERCLK(MHZ)
2.048MVIP non-multiplexed	2.048
4.096MHz non-multiplexed	4.096
8.192MHz non-multiplexed	8.192
12.352MHz Bit-multiplexed (DS1 ONLY)	12.352
16.384MHz Bit-multiplexed	16.384
16.384 HMVIP Byte-multiplexed	16.384
16.384 H.100 Byte-multiplexed	16.384

NOTES:

1. **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.*
2. *For DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSERCLK0/ RxLINECLK0	A6	D9	I/O	12	**(Continued)** **DS1 or E1 Framer Bypass Mode - RxLINECLKn** In this mode, RxSERCLKn is used as the Receive Line Clock output pin (RxLineClk) from the LIU. ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*
RxSERCLK1/ RxLINECLK1	B13	A12			
RxSERCLK2/ RxLINECLK2	C20	B18			
RxSERCLK3/ RxLINECLK3	H25	H20			
RxSERCLK4/ RxLINECLK4	AD26	W20			
RxSERCLK5/ RxLINECLK5	AC19	V16			
RxSERCLK6/ RxLINECLK6	AB12	W12			
RxSERCLK7/ RxLINECLK7	AB6	W6			
RxSER0/ RxPOS0	C7	B7	O	12	**Receive Serial Data Output (RxSERn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - RxSERn** These pins function as the receive serial data output on the system side interface, which are updated on the rising edge of the RxSERCLKn pin. All the framing alignment bits, facility data link bits, CRC bits, and signaling information will also be extracted to this output pin. **DS1 or E1 High-Speed Multiplexed Mode* - RxSERn** In this mode, these pins are used as the high-speed multiplexed data output pin on the system side. High-speed multiplexed data of channels 0-3 will output on RxSER0 and high-speed multiplexed data of channels 4-7 will output on RxSER4 in a byte or bit-interleaved way. The framer outputs the multiplexed data on RxSER0 and RxSER4 using the high-speed input clock (RxSERCLKn). **DS1 or E1 Framer Bypass Mode** In this mode, RxSERn is used as the positive digital output pin (RxPOSn) from the LIU. ***NOTE:*** **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*
RxSER1/ RxPOS1	B14	E14			
RxSER2/ RxPOS2	C21	D17			
RxSER3/ RxPOS3	D26	F20			
RxSER4/ RxPOS4	AC25	W19			
RxSER5/ RxPOS5	AC18	AA15			
RxSER6/ RxPOS6	AE12	AA9			
RxSER7/ RxPOS7	AB7	AB2			

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHN0_0/ RxSig0 RxCHN1_0/ RxSig1 RxCHN2_0/ RxSig2 RxCHN3_0/ RxSig3 RxCHN4_0/ RxSig4 RxCHN5_0/ RxSig5 RxCHN6_0/ RxSig6 RxCHN7_0/ RxSig7	D8 D14 A22 G26 AD25 AD18 AC13 AB8	A7 B13 B19 H19 AA22 U14 AA10 Y7	O	8	**Receive Time Slot Octet Identifier Output (RxCHNn_0) / Receive Serial Signaling Output (RxSIGn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_0:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_0 indicates the Least Significant Bit (LSB) of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxSIGn:** These pins can be used to output robbed-bit signaling data within an inbound DS1 frame or to output Channel Associated Signaling (CAS) data within an inbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel will be output on bit 4,5,6,7 of each time slot on the RxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel will be output on bit 4, 5 of each time slot on the RxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel will be output on bit 4 of each time slot on the RxSIG pin. **E1 Mode:** Signaling data in E1 mode will be output on the RxSIGn pins on a time-slot-basis as in T1 mode, or it can be output on time slot 16 only via the RxSIGn output pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 will be output on the RxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 will be output on the RxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) will be output on the RxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Receive Fractional/signaling interface can be enabled by programming to bit 4 - RxFr1544/ RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHN0_1/ RxFrTD0 RxCHN1_1/ RxFrTD1 RxCHN2_1/ RxFrTD2 RxCHN13_1/ RxFrTD3 RxCHN4_1/ RxFrTD4 RxCHN5_1/ RxFrTD5 RxCHN6_1/ RxFrTD6 RxCHN7_1/ RxFrTD7	E9 E14 B22 H26 AE25 AF18 AB13 AC7	C9 C13 C19 G21 AA21 AB16 V12 W8	O	8	**Receive Time Slot Octet Identifier Output Bit 1 (RxCHNn_1) / Receive Serial Fractional Output (RxFrTDn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_1:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_1 indicates Bit 1 of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxFrTDn:** These pins are used as the fractional data output pins to output fractional DS1/E1 payload data within an inbound DS1/E1 frame. In this mode, system equipment can use either RxCHCLK or RxSERCLK to clock out fractional DS1/E1 payload data depending on the framer configuration. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/ RxFr2048 bit from register 0xn122 to '1'.*
RxCHN0_2/ RxCHN0 RxCHN1_2/ RxCHN1 RxCHN2_2/ RxCHN2 RxCHN3_2/ RxCHN3 RxCHN4_2/ RxCHN4 RxCHN5_2/ RxCHN5 RxCHN6_2/ RxCHN6 RxCHN7_2/ RxCHN7	C9 A15 C22 J23 AF26 AB17 AF12 AF4	D10 D13 F17 J19 W18 AB15 AB9 Y4	O	8	**Receive Time Slot Octet Identifier Output-Bit 2 (RxCHNn_2) / Receive Time Slot Identifier Serial Output (RxCHNn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_2:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_2 indicates Bit 2 of the time slot channel being output. **If receive fractional/signaling interface is enabled - RxCHNn** These pins serially output the five-bit binary value of the time slot being output by the receive serial interface. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/ RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHN0_3/ Rx8KHZ0 RxCHN1_3/ Rx8KHZ1 RxCHN2_3/ Rx8KHZ2 RxCHN3_3/ Rx8KHZ3 RxCHN4_3/ Rx8KHZ4 RxCHN5_3/ Rx8KHZ5 RxCHN6_3/ Rx8KHZ6 RxCHN7_3/ Rx8KHZ7	C10 B16 C23 J26 AC23 AC17 AD12 AE5	E11 A15 D19 H21 AB22 V14 AB8 AA3	O	8	**Receive Time Slot Octet Identifier Output-Bit 3 (RxCHNn_3) / Receive 8KHz Clock Output (Rx8KHZn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_3:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_3 indicates Bit 3 of the time slot channel being output. **If receive fractional/signaling interface is enabled - Rx8KHZn:** These pins output a reference 8KHz clock signal derived from the MCLKIN input. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/ RxFr2048 bit from register 0xn122 to '1'.*
RxCHN0_4/ RxSCLK0 RxCHN1_4/ RxSCLK1 RxCHN2_4/ RxSCLK2 RxCHN3_4/ RxSCLK3 RxCHN4_4/ RxSCLK4 RxCHN5_4/ RxSCLK5 RxCHN6_4/ RxSCLK6 RxCHN7_4/ RxSCLK7	A10 C17 A26 K25 AB22 AD17 AF11 AF3	B10 F16 B21 J22 Y19 W14 AB7 W7	O	8	**Receive Time Slot Octet Identifier Output-Bit 4 (RxCHNn_4) / Receive Recovered Line Clock Output (RxSCLKn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled - RxCHNn_4:** These output pins (RxCHNn_4 through RxCHNn_0) reflect the five-bit binary value of the current time slot being output by the receive serial interface. System equipment can use the RxCHCLKn to sample the five output pins of each channel to identify the time slot being output on these pins. RxCHNn_4 indicates the Most Significant Bit (MSB) of the time slot channel being output. **If receive fractional/signaling interface is enabled - Receive Recovered Line Clock Output (RxSCLKn):** These pins output the recovered T1/E1 line clock (1.544MHz in T1 mode and 2.048MHz in E1 mode) for each channel. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/ RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCHCLK0 RxCHCLK1 RxCHCLK2 RxCHCLK3 RxCHCLK4 RxCHCLK5 RxCHCLK6 RxCHCLK7	A8 A14 A24 F25 AB24 AE21 AE11 AF5	E10 E15 B20 G19 U18 AB19 AA8 Y5	O	8	**Receive Channel Clock Output (RxCHCLKn):** The exact function of this pin depends on whether or not the receive framer enables the receive fractional/signaling interface to output fractional data, as described below. **If receive fractional/signaling interface is disabled:** This pin indicates the boundary of each time slot of an inbound DS1/E1 frame. In T1 mode, each of these output pins is a 192kHz clock which pulses "High" during the LSB of each 24 time slots. In E1 mode, each of these output pins is a 256kHz clock which pulses "High" during the LSB of each 32 time slots. System Equipment can use this clock signal to sample the RxCHN0 through RxCHN4 time slot identifier pins to determine which time slot is being output. **If receive fractional/signaling interface is enabled:** RxCHCLKn is the fractional interface clock which either outputs a clock signal for the time slot that has been configured to output fractional data, or outputs an enable signal for the fractional time slot so that fractional data can be clocked out of the device using the RxSERCLK pin. ***NOTE:*** *Receive fractional interface can be enabled by programming to bit 4 - RxFr1544/RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE LINE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RTIP0 RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7	D1 F1 H1 K1 M1 P1 T1 V1	G2 H2 K4 L2 M2 P3 T2 U4	I	-	**Receive Positive Analog Input (RTIPn):** RTIP is the positive differential input from the line interface. This input pin, along with the RRING input pin, functions as the "Receive DS1/E1 Line Signal" input for the XRT86VL38 device. The user is expected to connect this signal and the RRING input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side) to improve long haul application receive capabilities.
RRING0 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7	E1 G1 J1 L1 N1 R1 U1 W1	G3 H1 K3 L1 M1 P2 T3 U3	I	-	**Receive Negative Analog Input (RRINGn):** RRING is the negative differential input from the line interface. This input pin, along with the RTIP input pin, functions as the "Receive DS1/E1 Line Signal" input for the XRT86VL38 device. The user is expected to connect this signal and the RTIP input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1µF to ground (Chip Side) to improve long haul application receive capabilities.
RxLOS_0 RxLOS_1 RxLOS_2 RxLOS_3 RxLOS_4 RxLOS_5 RxLOS_6 RxLOS_7	E8 A16 B20 H24 AC26 AF20 AC12 AD4	C8 C14 D16 F22 W21 W15 Y10 U8	O	4	**Receive Loss of Signal Output Indicator (RLOSn):** The XRT86VL38 device will assert this output pin (i.e., toggle it "high") anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block declares the LOS defect condition. Conversely, the XRT86VL38 device will negate this output pin (i.e., toggle it "low") anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block is NOT declaring the LOS defect condition. This output pin will toggle "High" (declare LOS) if the Receive Framer or the Receive LIU block associated with Channel N determines that an RLOS condition occurs. In other words, this pin is OR-ed with the LIU RLOS and the Framer RLOS bit. If either the LIU RLOS or the Framer RLOS bit associated with channel N pulses high, the corresponding RLOS pin of that particular channel will be set to "High".

RECEIVE LINE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxTSEL	D5	C6	I	-	**Receive Termination Control (RxTSEL):** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register (0x0FE2). Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.* **RxTSEL (pin)** / **Rx Termination** 0 / External 1 / Internal *Note: RxTCNTL (bit) must be set to "1"*

TRANSMIT LINE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	DESCRIPTION
TTIP0 TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7	F3 G3 J3 K3 M3 P3 T3 U3	F3 H4 J3 K1 M5 N2 R4 T1	O	**Transmit Positive Analog Output (TTIPn):** TTIP is the positive differential output to the line interface. This output pin, along with the corresponding TRING output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VL38 device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. This output pin will be tri-stated whenever the user sets the “TxON” input pin or register bit (0xnF02, bit 3) to “0”. ***NOTE:*** *This pin should have a series line capacitor of 0.68μF for DC blocking purposes.*
TRING0 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7	G4 H4 K4 L4 M4 P4 R4 U4	F1 J5 J1 L4 M3 P5 R2 U2	O	**Transmit Negative Analog Output (TRINGn):** TRING is the negative differential output to the line interface. This output pin, along with the corresponding TTIP output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VL38 device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the “TxON” input pin or register bit (0xnF02, bit 3) to “0”.*

TRANSMIT LINE INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	DESCRIPTION
TxON	Y3	W1	I	**Transmitter On** This input pin permits the user to either enable or disable the Transmit Output Driver within the Transmit DS1/E1 LIU Block. If the TxON pin is pulled "Low", all 8 Channels are tri-stated. When this pin is pulled 'High', turning on or off the transmitters will be determined by the appropriate channel registers (address 0x0Fn2, bit 3) **LOW** = Disables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the TTIP and TRING output pins of all 8 channels will be tri-stated. **HIGH** = Enables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the corresponding TTIP and TRING output pins will be enabled or disabled by programming the appropriate channel register. (address 0x0Fn2, bit 3) ***NOTE:*** *Whenever the transmitters are turned off, the TTIP and TRING output pins will be tri-stated.*

TIMING INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
MCLKIN	A4	A5	I	-	**Master Clock Input:** This pin is used to provide the timing reference for the internal master clock of the device. The frequency of this clock is programmable from 8kHz to 16.384MHz in register 0x0FE9.
E1MCLKnOUT	B5	A4	O	12	**LIU E1 Output Clock Reference** This output pin is defaulted to 2.048MHz, but can be programmed to 4.096MHz, 8.192MHz, or 16.384MHz in register 0x0FE4.
T1MCLKnOUT	D6	F9	O	12	**LIU T1 Output Clock Reference** This output pin is defaulted to 1.544MHz, but can be programmed to output 3.088MHz, 6.176MHz, or 12.352MHz in register 0x0FE4.
E1OSCCLK	Y5	V4	O	8	**Framer E1 Output Clock Reference** This output pin is defaulted to 2.048MHz, but can be programmed to 65.536MHz in register 0x011E.
T1OSCCLK	AC1	V3	O	8	**Framer T1 Output Clock Reference** This output pin is defaulted to 1.544MHz, but can be programmed to output 49.408MHz in register 0x011E.
8KSYNC	AB3	W2	O	8	**8kHz Clock Output Reference** This pin is an output reference of 8kHz based on the MCLKIN input. Therefore, the duty cycle of this output is determined by the time period of the input clock reference.

TIMING INTERFACE

SIGNAL NAME	420 PKG BALL#	484 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
8KEXTOSC	AA2	U5	I	-	**External Oscillator Select** For normal operation, this pin should not be used, or pulled "Low". This pin is internally pulled "Low" with a 50kΩ resistor.
ANALOG	C5	D4	O		**Factory Test Mode Pin** ***NOTE:*** *For Internal Use Only*
LOP	AB1	V2	I	-	**Loss of Power for E1 Only** This is a Loss of Power pin in the E1 application only. Upon detecting LOP in E1 mode, the device will automatically transmit the Sa5 and Sa6 bit to a different pattern, so that the Receive terminal can detect a power failure in the network. Please see register 0xn131 for the Transmit SA control.
SENSE	E6	E6	O		***NOTE:*** *For Internal Use Only*

GPIO INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
GPIO1_3 GPIO1_2 GPIO1_1 GPIO1_0	B21 G22 AE24 AE22	A19 G18 AA20 AA18	I/O	8	**General Purpose Input/Output Pins** Each of these pins can be configured to function as either a general-purpose input or output pin. The exact function of these pins depend on whether these GPIO pins are configured as input or output pins as follows. **If GPIO1_n pins are configured as input pins:** The state of these input pins can be monitored by reading the GPIO1_n Control Bits (Bit 3-0) within the "General Purpose Input/Output 1 Control Register (address 0x4102). **If GPIO1_n pins are configured as output pins:** The state of these output pins can be controlled by writing the appropriate value into the GPIO1_n Control Bits (Bit 3-0) within the "General Purpose Input/Output 1 Control Register (address 0x4102). Finally, users can configure a given GPIO1_n pin to be an input pin by setting the corresponding GPIO1_nDIR Bit (from Bit 7-4), within the "General Purpose Input/Output 1 Control Register (address 0x4102) to '0'. Conversely, users can configure the GPIO1_ n pin to be an output pin by setting the corresponding GPIO1_nDIR Bit (from Bit 7-4), within the "General Purpose Input/Output 1 Control Register (address 0x4102) to '1'.
GPIO0_3 GPIO0_2 GPIO0_1 GPIO0_0	AD20 AB18 AD13 AD11	U16 V15 Y11 AB6	I/O	8	**General Purpose Input/Output Pins** Each of these pins can be configured to function as either a general-purpose input or output pin. The exact function of these pins depend on whether these GPIO pins are configured as input or output pins as follows. **If GPIO0_n pins are configured as input pins:** The state of these input pins can be monitored by reading the GPIO0_n Control Bits (Bit 3-0) within the "General Purpose Input/Output 0 Control Register (address 0x0102). **If GPIO0_n pins are configured as output pins:** The state of these output pins can be controlled by writing the appropriate value into the GPIO0_n Control Bits (Bit 3-0) within the "General Purpose Input/Output 0 Control Register (address 0x0102). Finally, users can configure a given GPIO0_n pin to be an input pin by setting the corresponding GPIO0_nDIR Bit (from Bit 7-4), within the "General Purpose Input/Output 0 Control Register (address 0x0102) to '0'. Conversely, users can configure the GPIO0_ n pin to be an output pin by setting the corresponding GPIO0_nDIR Bit (from Bit 7-4), within the "General Purpose Input/Output 0 Control Register (address 0x0102) to '1'.

JTAG INTERFACE

The XRT86VL38 device's JTAG features comply with the IEEE 1149.1 standard. Please refer to the industry specification for additional information on boundary scan operations.

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
TCK	A7	F10	I	-	**Test clock: Boundary Scan Test clock input:** The TCLK signal is the clock for the TAP controller, and it generates the boundary scan data register clocking. The data on TMS and TDI is loaded on the positive edge of TCK. Data is observed at TDO on the falling edge of TCK.
TMS	A5	B6	I	-	**Test Mode Select:** Boundary Scan Test Mode Select input. The TMS signal controls the transitions of the TAP controller in conjunction with the rising edge of the test clock (TCK). ***NOTE:*** *For normal operation this pin must be pulled 'High'.*
TDI	D7	E9	I	-	**Test Data In:** Boundary Scan Test data input The TDI signal is the serial test data input. ***NOTE:*** *This pin is internally pulled 'high'.*
TDO	B6	D8	O	8	**Test Data Out:** Boundary Scan Test data output The TDO signal is the serial test data output.
TRST	B7	A6	I	-	**Test Reset Input:** The TRST signal (Active Low) asynchronously resets the TAP controller to the Test-Logic-Reset state. ***NOTE:*** *This pin is internally pulled 'high'*
TEST	B11	E12	I	-	**Factory Test Mode Pin** ***NOTE:*** *This pin is internally pulled 'low', and should be pulled 'low' for normal operation.*
aTEST	E7	C7	I	-	**Factory Test Mode Pin** ***NOTE:*** *This pin is internally pulled 'low', and should be pulled 'low' for normal operation.*
JTAG_Ring	D4	C2	I	-	**JTAG_Ring Test Pin**
JTAG_Tip	F5	E5	I	-	**JTAG_Tip Test Pin**

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	Y26 W24 T25 T26 P24 N25 N24 M25	T19 U20 P21 N18 M22 M20 M21 L21	I/O	8	**Bidirectional Microprocessor Data Bus** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ or WRITE operations with the Microprocessor Interface of the XRT86VL38 device. When DMA interface is enabled, these 8-bit bidirectional data bus is also used by the T1/E1 Framer or the external DMA Controller for storing and retrieving information.
$\overline{\text{REQ0}}$	AB26	U19	O	8	**DMA Cycle Request Output—DMA Controller 0 (Write)**: These output pins are used to indicate that DMA transfers (Write) are requested by the T1/E1 Framer. On the transmit side (i.e., To transmit data from external DMA controller to HDLC buffers within the XRT86VL38), DMA transfers are only requested when the transmit buffer status bits indicate that there is space for a complete message or cell. The DMA Write cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{\text{REQ0}}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{\text{ACK0}}$) 'low' to indicate that it is ready to start the transfer. The external DMA controller should place new data on the Microprocessor data bus each time the Write Signal is Strobed low if the $\overline{\text{WR}}$ is configured as a Write Strobe. If $\overline{\text{WR}}$ is configured as a direction signal, then the external DMA controller would place new data on the Microprocessor data bus each time the Read Signal ($\overline{\text{RD}}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when at least one of the Transmit HDLC buffers are empty and can receive one more HDLC message. The Framer negates this output pin (toggles it "High") when the HDLC buffer can no longer receive another HDLC message.

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{\text{REQ1}}$	AA24	Y22	O	8	**DMA Cycle Request Output—DMA Controller 1 (Read):** These output pins are used to indicate that DMA transfers (Read) are requested by the T1/E1 Framer. On the receive side (i.e., To transmit data from HDLC buffers within the XRT86VL38 to external DMA Controller), DMA transfers are only requested when the receive buffer contains a complete message or cell. The DMA Read cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{\text{REQ1}}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{\text{ACK1}}$) 'low' to indicate that it is ready to receive the data. The T1/E1 Framer should place new data on the Microprocessor data bus each time the Read Signal is Strobed low if the $\overline{\text{RD}}$ is configured as a Read Strobe. If $\overline{\text{RD}}$ is configured as a direction signal, then the T1/E1 Framer would place new data on the Microprocessor data bus each time the Write Signal ($\overline{\text{WR}}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when one of the Receive HDLC buffer contains a complete HDLC message that needs to be read by the µC/µP. The Framer negates this output pin (toggles it "High") when the Receive HDLC buffers are depleted.
$\overline{\text{INT}}$	R26	N22	O	8	**Interrupt Request Output:** This active-low output signal will be asserted when the XRT86VL38 device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the Microprocessor. The Framer will assert this active "Low" output (toggles it "Low"), to the local µP, anytime it requires interrupt service.

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
PCLK	Y25	V22	I	-	**Microprocessor Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in this mode, then it will use this clock signal to do the following. **1.** To sample the $\overline{CS}$, $\overline{WR}$/R/$\overline{W}$, A[14:0], D[7:0], $\overline{RD}$/$\overline{DS}$ and DBEN input pins, and **2.** To update the state of the D[7:0] and the RDY/DTACK output signals. ***NOTES:*** *1. The Microprocessor Interface can work with PCLK frequencies ranging up to 33MHz.* *2. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronous Modes. In this case, the user should tie this pin to GND.* When DMA interface is enabled, the PCLK input pin is also used by the T1/E1 Framer to latch in or latch out receive or output data respectively.
iADDR	W22	R18	I	-	**This Pin Must be Tied "Low" for Normal Operation.** This pin is internally pulled "High" with a 50kΩ resistor.
fADDR	AA26	T18	I	-	**This Pin Must be Tied "High" for Normal Operation.** This pin is internally pulled "Low" with a 50kΩ resistor.
PTYPE0 PTYPE1 PTYPE2	W23 W26 R25	V20 T20 N21	I	-	**Microprocessor Type Input:** These input pins permit the user to specify which type of Microprocessor/Microcontroller to be interfaced to the XRT86VL38 device. The following table presents the three different microprocessor types that the XRT86VL38 supports. **µPType2 / µPType1 / µPType0 / MICROPROCESSOR TYPE** 0 0 0 — 68HC11, 8051, 80C188 0 0 1 — MOTOROLA 68K 1 0 1 — IBM POWER PC 403 ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{RDY}$	V24	R19	O	12	**Ready/Data Transfer Acknowledge Output:** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VL38 has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel Asynchronous Mode - $\overline{RDY}$ - Ready Output** Tis output pin will function as the “active-low” READY output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level. **Motorola Asynchronous Mode - $\overline{DTACK}$ - Data Transfer Acknowledge Output** Tis output pin will function as the “active-low” DTACK output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{RDY}$	V24	R19	O	12	**(Con't)** **Power PC 403 Mode - RDY Ready Output:** This output pin will function as the "active-high" READY output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at the logic "high" level upon the rising edge of PCLK, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "low" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it samples this output pin being at the logic low level. ***NOTE:*** *The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.*
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14	V25 V26 U22 U23 U24 U25 U26 T22 T24 R23 R24 P22 P25 N23 N22	P18 N17 T21 T22 R20 R21 R22 P19 P20 N19 N20 M18 M19 L18 L22	I	-	**Microprocessor Interface Address Bus Input** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations within the XRT86VL38 device whenever it performs READ and WRITE operations with the XRT86VL38 device. ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor, except ADDR[8:14].*
$\overline{DBEN}$	V23	U22	I	-	**Data Bus Enable Input pin.** This active-low input pin permits the user to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. • Setting this input pin "low" enables the Bi-directional Data bus. • Setting this input pin "high" tri-states the Bi-directional Data Bus.

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
ALE	R22	P22	I	-	**Address Latch Enable Input Address Strobe** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VL38 has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - ALE** This active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[14:0]) into the XRT86VL38 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "high" enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT86VL38 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - $\overline{\text{AS}}$** This active-low input pin is used to latch the data residing on the Address Bus, A[14:0] into the Microprocessor Interface circuitry of the XRT86VL38 device. Pulling this input pin "low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **Power PC 403 Mode - No Function -Tie to GND:** This input pin has no role nor function and should be tied to GND.
$\overline{\text{CS}}$	L26	K21	I	-	**Microprocessor Interface—Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT86VL38 on-chip registers and buffer/memory locations.

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{RD}$	W25	U21	I	-	**Microprocessor Interface—Read Strobe Input:** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the Framer has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - $\overline{RD}$ - READ Strobe Input:** This input pin will function as the **$\overline{RD}$** (Active Low Read Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT86VL38 device will place the contents of the addressed register (or buffer location) on the Microprocessor Interface Bi-directional data bus (D[7:0]). When this signal is negated, then the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode - $\overline{DS}$ - Data Strobe:** This input pin will function as the $\overline{DS}$ (Data Strobe) input signal. **Power PC 403 Mode - $\overline{WE}$ - Write Enable Input:** This input pin will function as the $\overline{WE}$ (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with $\overline{CS}$ and $\overline{WR}$/R/$\overline{W}$) also being asserted (at a logic low level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the "target" on-chip register or buffer location within the XRT86VL38 device.
$\overline{WR}$	M23	L20	I	-	**Microprocessor Interface—Write Strobe Input** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VL38 has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - $\overline{WR}$ - Write Strobe Input:** This input pin functions as the $\overline{WR}$ (Active Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pin, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT86VL38) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - R/$\overline{W}$ - Read/Write Operation Identification Input Pin:** This pin is functionally equivalent to the "R/$\overline{W}$" input pin. In the Motorola Mode, a "READ" operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin. Similarly a WRITE operation occurs if this pin is at a logic "0", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin.

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{WR}$	M23	L20	I	-	**(Con't)** **Power PC 403 Mode - R/$\overline{W}$ - Read/Write Operation Identification Input:** This input pin will function as the "Read/Write Operation Identification Input" pin. Anytime the Microprocessor Interface samples this input signal at a logic "High" (while also sampling the $\overline{CS}$ input pin "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the $\overline{DBEN/OE}$ input pin, and the Microprocessor Interface will then place the contents of the "target" register (or address location within the XRT86VL38 device) upon the Bi-Directional Data Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic "Low" (while also sampling the $\overline{CS}$ input pin a logic "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the $\overline{RD/DS/WE}$ input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the "target" register or buffer location (within the XRT86VL38).

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{ACK0}$	Y23	W22	I	-	**DMA Cycle Acknowledge Input—DMA Controller 0 (Write):** The external DMA Controller will assert this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_0 output signal. **2.** When the external DMA Controller is ready to transfer data from external memory to the selected Transmit HDLC buffer. At this point, the DMA transfer between the external memory and the selected Transmit HDLC buffer may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req_0}$ output pin. The external DMA Controller must do this in order to acknowledge the end of the DMA cycle. **DMA Cycle Acknowledge Input—DMA Controller 1 (Read):** The external DMA Controller asserts this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_1 output signal. **2.** When the external DMA Controller is ready to transfer data from the selected Receive HDLC buffer to external memory. At this point, the DMA transfer between the selected Receive HDLC buffer and the external memory may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req_1}$ output pin. The external DMA Controller will do this in order to acknowledge the end of the DMA cycle. ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor.*
$\overline{ACK1}$	Y24	V21			

MICROPROCESSOR INTERFACE

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{\text{BLAST}}$	P23	M17	I	-	**Last Cycle of Burst Indicator Input:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. ***NOTES:*** *1. If the user has configured the Microprocessor Interface to operate in the Intel-Asynchronous, the Motorola-Asynchronous or the Power PC 403 Mode, then he/she should tie this input pin to GND.* *2. This pin is internally pulled "High" with a 50kΩ resistor.*
$\overline{\text{RESET}}$	Y4	Y1	I	-	**Hardware Reset Input** $\overline{\text{Reset}}$ is an active low input. If this pin is pulled "Low" for more than 10µS, the device will be reset. When this occurs, all output will be 'tri-stated', and all internal registers will be reset to their default values.

POWER SUPPLY PINS (3.3V)

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	DESCRIPTION
VDD	Y2 AC4 AC11 AE18 AD23 AA25 N26 F24 A25 C15 C8	G10 G12 G15 H17 L16 R17 T7 T9 T11 T13 T15	PWR	**Framer Block Power Supply (I/O)**
RVDD	D2 F2 H2 K2 M2 P2 T2 V2	E1 H5 K6 L6 M7 N4 R5 T5	PWR	**Receiver Analog Power Supply for LIU Section**

POWER SUPPLY PINS (3.3V)

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	DESCRIPTION
TVDD	F4 H3 J4 L3 N3 R3 T4 V3	F2 G1 J2 L3 M6 N1 R3 U1	PWR	**Transmitter Analog Power Supply for LIU Section**

POWER SUPPLY PINS (1.8V)

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	DESCRIPTION
VDD18	AD1 AD7 AF14 AB20 AC24 T23 J24 D24 E18 E12	G11 G14 G16 J17 P17 T8 T10 T12 T14 T17	PWR	**Framer Block Power Supply**
DVDD18	A1	F5	PWR	**Digital Power Supply for LIU Section**
AVDD18	B4	A2	PWR	**Analog Power Supply for LIU Section**
VDDPLL18	D3 C2 B1 C1	B1 C1 D2 E3	PWR	**Analog Power Supply for PLL**

GROUND PINS

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	DESCRIPTION
VSS	Y1 AA1 AE2 AD6 AD9 AF13 AC16 AB19 AC22 AB23 AA23 V22 P26 L23 H22 C25 B25 D20 B17 C13 D10 C06	F6 G6 G7 G8 G9 G13 H6 H7 H16 J7 J16 K7 K16 L7 M16 N6 N7 N16 P6 P7 P16 R6 R7 R16 T6 T16 U6 H8-H15 J8-J15 K8-K15 L8-L15 M8-M15 N8-N15 P8-P15 R8-R15	GND	**Framer Block Ground**
DGND	A2	B5	GND	**Digital Ground for LIU Section**
AGND	A3	B3	GND	**Analog Ground for LIU Section**

GROUND PINS

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	DESCRIPTION
RGND	E2 G2 J2 L2 N2 R2 U2 W2	F4 H3 J4 K2 M4 N3 P1 T4	GND	**Receiver Analog Ground for LIU Section**
TGND	H5 J5 K5 L5 M5 N5 R5 T5	G4 J6 K5 L5 N5 P4 R1 V1	GND	**Transmitter Analog Ground for LIU Section**
GNDPLL18	C3 E4 E3 B2	D3 E4 D1 E2	GND	**Analog Ground for PLL**

NO CONNECT PINS

SIGNAL NAME	420 PKG BALL#	484PKG BALL #	TYPE	DESCRIPTION
NC	B3 B18 B23 C4 D23 E5 E16 E19 E22 G5 N4 P5 U5 V4 V5 W3 W4 W5 AA3 AA4 AA5 AF1	A1 A3 A22 B2 C3 C4 C5 D5 D6 D7 E7 E8 F7 F8 G5 B4 F18	NC	**No Connection**

ELECTRICAL CHARACTERISTICS

Absolute Maximums

Power Supply.....		Power Rating STBGA and PBGA Package..... 2.4
VDD_{IO} .. .. -0.5V to +3.465V		
VDD_{CORE}.....-0.5V to +1.890V		
Storage Temperature .....-65°C to 150°C		Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V
Operating Temperature Range.....-40°C to 85°C		ESD Protection (HBM).....>2000V
Supply Voltage ..... GND-0.5V to +VDD + 0.5V		Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LL}	Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{IL}	Input Low voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VDD	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = -1.6mA
VOH	Output High Voltage	TBD		VDD	V	
I_{OC}	Open Drain Output Leakage Current				µA	
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND

XRT86VL38 POWER CONSUMPTION

Test Conditions: TA = 25°C, VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, Internal termination, unless otherwise specified

MODE	IMPEDANCE	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T1	100Ω		2.21		W	QRSS Pattern with All 8 Channels on
E1	75Ω		2.07		W	QRSS Pattern with All 8 Channels on
E1	120Ω		1.93		W	QRSS Pattern with All 8 Channels on

TABLE 4: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A= -40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					Cable attenuation @1024kHz
Number of consecutive zeros before RLOS is set		32			
Input signal level at RLOS	15	20		dB	ITU-G.775, ETSI 300 233
RLOS De-asserted	12.5			% ones	
Receiver Sensitivity (Short Haul with cable loss)	11			dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Receiver Sensitivity (Long Haul with cable loss)	0		43	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Input Impedance		15		kΩ	
Input Jitter Tolerance: 1 Hz 10kHz-100kHz	 37 0.3			 UIpp UIpp	ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 -	 20	 0.5	 kHz dB	ITU G.736
Jitter Attenuator Corner Frequency (-3dB curve) (JABW=0) (JABW=1)	-	10 1.5	-	Hz Hz	ITU G.736
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 12 8 8	-	-	 dB dB dB	ITU-G.703

TABLE 5: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					
Number of consecutive zeros before RLOS is set		175			
Input signal level at RLOS	15	20	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss)		-			With nominal pulse amplitude of 3.0V for 100Ω termination
Normal	0		36	dB	
Extended	0		45	dB	
Input Impedance		15	-	kΩ	
Jitter Tolerance:					
1Hz	138	-	-	UIpp	AT&T Pub 62411
10kHz - 100kHz	0.4	-	-		
Recovered Clock Jitter					
Transfer Corner Frequency	-	10	-	KHz	TR-TSY-000499
Peaking Amplitude	-		0.1	dB	
Jitter Attenuator Corner Frequency (-3dB curve)	-	6		Hz	AT&T Pub 62411
Return Loss:					
51kHz - 102kHz	-	14	-	dB	
102kHz - 2048kHz	-	20	-	dB	
2048kHz - 3072kHz	-	16	-	dB	

TABLE 6: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:					1:2 transformer
75Ω Application	2.13	2.37	2.60	V	
120Ω Application	2.70	3.00	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703

TABLE 6: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss:					
51kHz -102kHz	15	-	-	dB	ETSI 300 166
102kHz-2048kHz	9	-	-	dB	
2048kHz-3072kHz	8	-	-	dB	

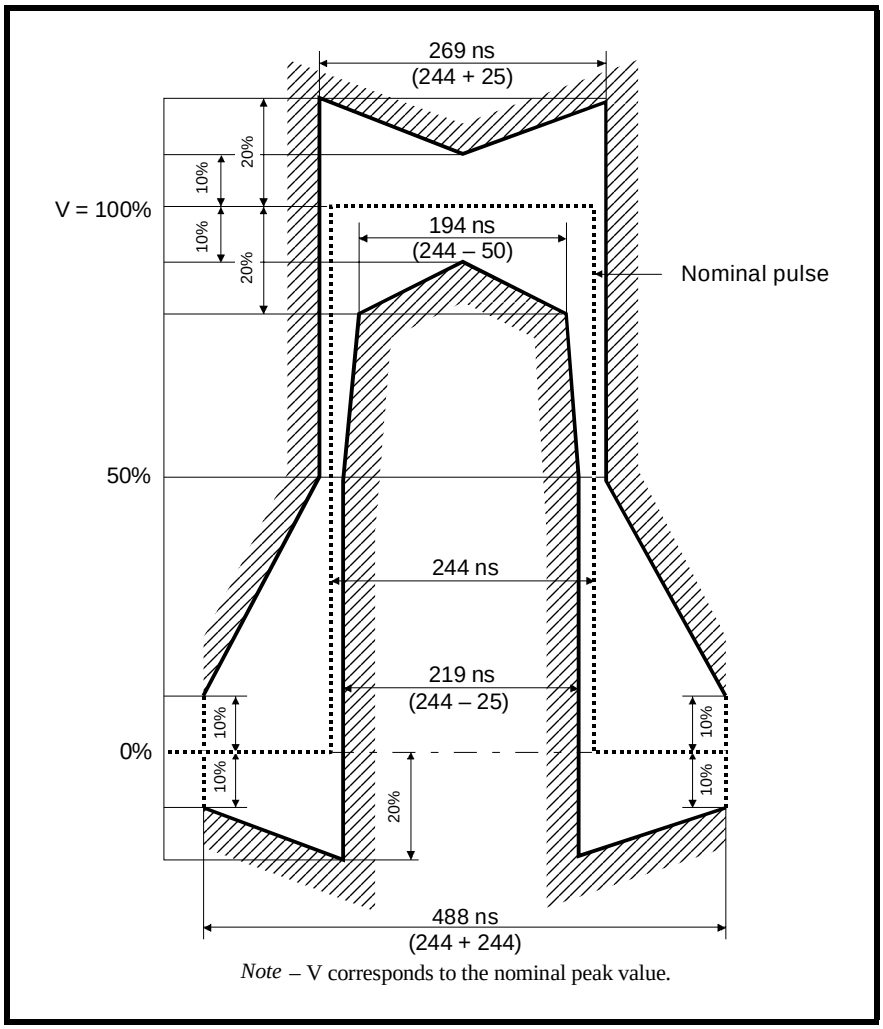
TABLE 7: E1 TRANSMIT RETURN LOSS REQUIREMENT

FREQUENCY	RETURN LOSS ETS 300166
51-102kHz	6dB
102-2048kHz	8dB
2048-3072kHz	8dB

TABLE 8: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:	2.4	3.0	3.60	V	1:2 transformer measured at DSX-1.
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss:					
51kHz -102kHz	-	17	-	dB	
102kHz-2048kHz	-	12	-	dB	
2048kHz-3072kHz	-	10	-	dB	

FIGURE 2. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

TABLE 9: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Nominal Peak Voltage of a Mark	2.37V	3.0V
Peak voltage of a Space (no Mark)	0 ± 0.237V	0 ± 0.3V
Nominal Pulse width	244ns	244ns
Ratio of Positive and Negative Pulses Imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 3. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

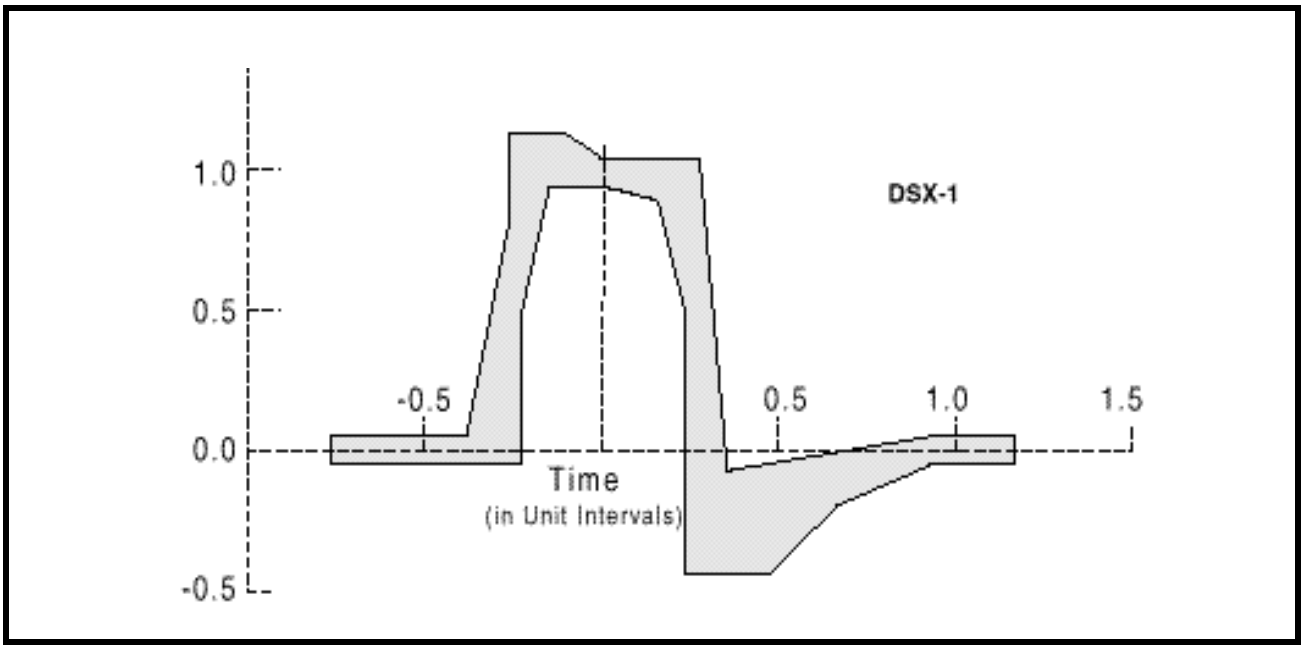


TABLE 10: DSX1 INTERFACE ISOLATED PULSE MASK AND CORNER POINTS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE	TIME (UI)	NORMALIZED AMPLITUDE
-0.77	-.05V	-0.77	.05V
-0.23	-.05V	-0.39	.05V
-0.23	0.5V	-0.27	.8V
-0.15	0.95V	-0.27	1.15V
0.0	0.95V	-0.12	1.15V
0.15	0.9V	0.0	1.05V
0.23	0.5V	0.27	1.05V
0.23	-0.45V	0.35	-0.07V
0.46	-0.45V	0.93	0.05V
0.66	-0.2V	1.16	0.05V
0.93	-0.05V		
1.16	-0.05V		

TABLE 11: AC ELECTRICAL CHARACTERISTICS

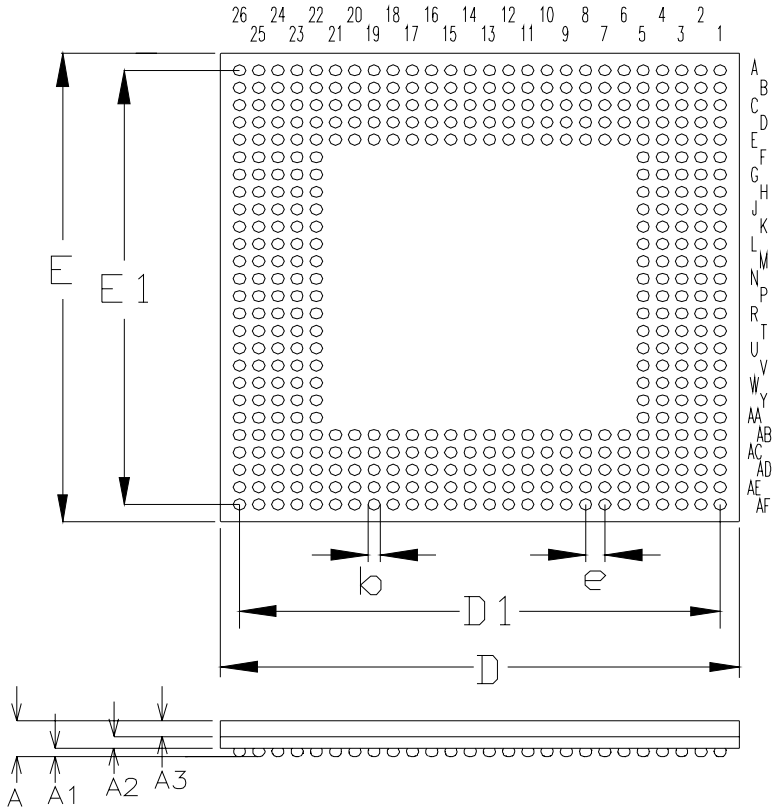
VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, TA=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
MCLKIN Clock Duty Cycle		40	-	60	%
MCLKIN Clock Tolerance		-	±50	-	ppm

ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL38IB	420 Plastic Ball Grid Array	-40°C to +85°C
XRT86VL38IB484	484 Shrink Thin Ball Grid Array	-40°C to +85°C

PACKAGE DIMENSIONS FOR 420 PLASTIC BALL GRID ARRAY

420 Plastic Ball Grid Array
(35.0 mm x 35.0 mm, PBGA)
Rev. 1.00

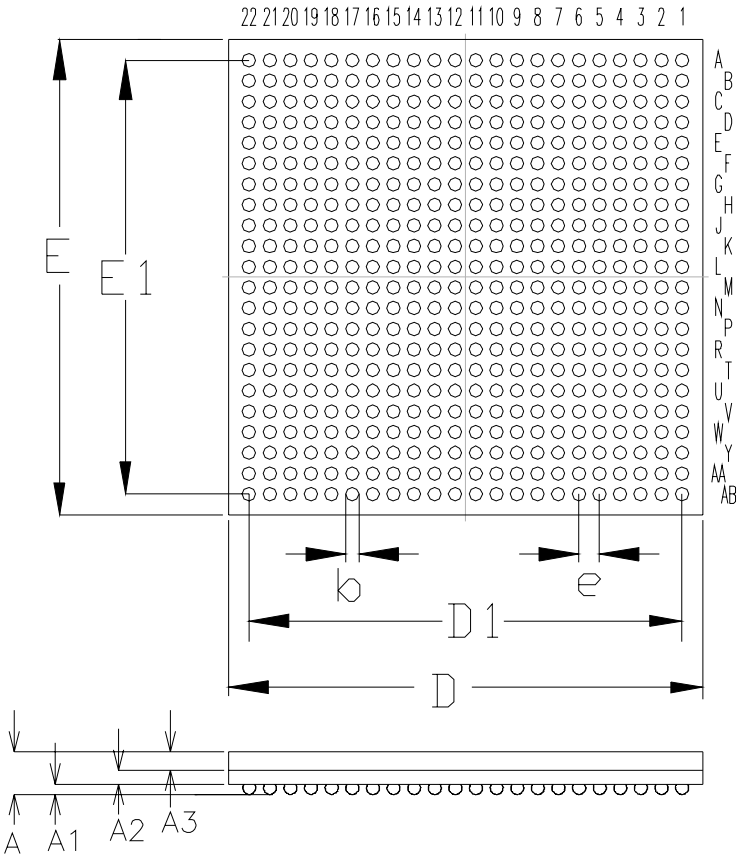


Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.085	0.098	2.16	2.50
A1	0.020	0.028	0.50	0.70
A2	0.020	0.024	0.51	0.61
A3	0.045	0.047	1.15	1.19
D	1.370	1.386	34.80	35.20
D1	1.2500 BSC		31.75 BSC	
E	1.370	1.386	34.80	35.20
E1	1.2500 BSC		31.75 BSC	
b	0.024	0.035	0.60	0.90
e	0.0500 BSC		1.27 TYP.	

PACKAGE DIMENSIONS FOR 484 SHRINK THIN BALL GRID ARRAY

484 Shrink Thin Ball Grid Array
(23.0 mm x 23.0 mm, STBGA)
Rev. 1.00



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.071	0.082	1.80	2.08
A1	0.019	0.022	0.47	0.57
A2	0.019	0.022	0.48	0.56
A3	0.033	0.037	0.85	0.95
D	0.898	0.913	22.80	23.20
D1	0.8268 BSC		21.00 BSC	
E	0.898	0.913	22.80	23.20
E1	0.8268 BSC		21.00 BSC	
b	0.024	0.028	0.60	0.70
e	0.0394 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
V1.2.0	January 29, 2007	Released to production.

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