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July 2014

FXMA2102
Dual Supply, 2-Bit Voltage Translator / Buffer / Repeater / Isolator for I²C Applications

Features

- Bi-Directional Interface between Any Two Levels: 1.65 V to 5.5 V
- Direction Control not Needed
- System GPIO Resources Not Required when OE Tied to V_{CCA}
- I²C 400 pF Buffer / Repeater
- I²C Bus Isolation
- A/B Port V_{OL} = 175 mV (Typical), V_{IL} = 150 mV, I_{OL} = 6 mA
- Open-Drain Inputs / Outputs
- Accommodates Standard-Mode and Fast-Mode I²C-Bus Devices
- Supports I²C Clock Stretching & Multi-Master
- Fully Configurable: Inputs and Outputs Track V_{CC}
- Control Input (/OE) Referenced to V_{CCA}.
- Non-Preferential Power-Up; Either V_{CC} May Be Powered-Up First
- Outputs Switch to 3-State if Either V_{CC} is at GND
- Tolerant Output Enable: 5 V
- Packaged in 8-Terminal Leadless MicroPak™ (1.6 mm x 1.6 mm) and Ultrathin MLP (1.2 mm x 1.4 mm)
- ESD Protection Exceeds:
  - 8 kV HBM ESD (per JESD22-A114)
  - 2 kV CDM (per JESD22-C101)

Description

The FXMA2102 is a high-performance configurable dual-voltage-supply translator for bi-directional voltage translation over a wide range of input and output voltages levels.

Intended for use as a voltage translator between I²C-Bus® complaint masters and slaves.

The device is designed so that the A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional A/B port voltage translation between any two levels from 1.65 V to 5.5 V. V_{CCA} can equal V_{CCB} from 1.65V to 5.5V. The OE pin is referenced to V_{CCA}.

Either V_{CC} can be powered-up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The two ports of the device have automatic direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FXMA2102L8X	-40 to +85°C	XN	8-Lead MicroPak™, 1.6 mm Wide	5000 Units on Tape and Reel
FXMA2102UMX			8-Lead Ultrathin MLP, 1.2 mm x 1.4 mm	

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Block Diagram

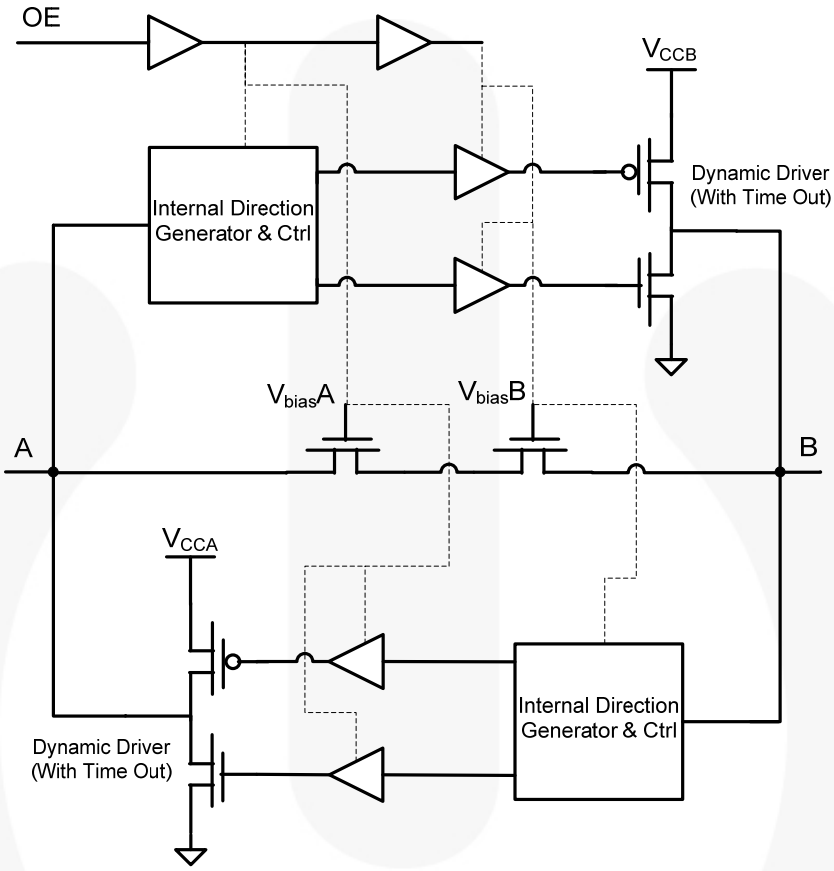

Figure 1. Block Diagram, 1 of 2 Channels

Pin Configuration

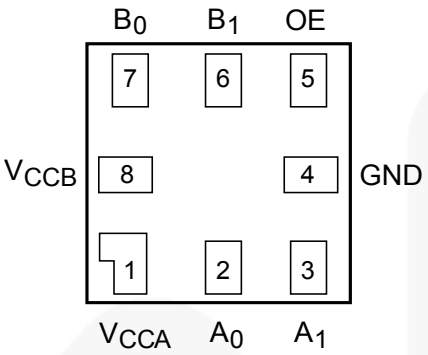

Figure 2. MicroPak™ (Top-Through View)

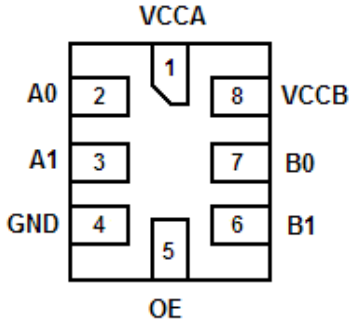

Figure 3. UMLP (Top-Through View)

Pin Definitions

Pin #	Name	Description
1	V_{CCA}	A-Side Power Supply
2, 3	A_0, A_1	A-Side Inputs or 3-State Outputs
4	GND	Ground
5	OE	Output Enable Input (Referenced to V_{CCA})
6, 7	B_1, B_0	B-Side Inputs or 3-State Outputs
8	V_{CCB}	B-Side Power Supply

Truth Table

Control	Outputs
OE	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

Note:

1. If the OE pin is driven LOW, the FXMA2102 is disabled and the A_0, A_1, B_0, and B_1 pins (including dynamic drivers) are forced into 3-state.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CCA}, V_{CCB}	Supply Voltage		–0.5	7.0	V
V_{IN}	DC Input Voltage	A Port	–0.5	7.0	
		B Port	–0.5	7.0	
		Control Input (OE)	–0.5	7.0	
V_O	Output Voltage[2]	A_n Outputs 3-State	–0.5	7.0	V
		B_n Outputs 3-State	–0.5	7.0	
		A_n Outputs Active	–0.5	V_{CCA} + 0.5V	
		B_n Outputs Active	–0.5	V_{CCB} + 0.5V	
I_{IK}	DC Input Diode Current	At V_{IN} < 0 V		–50	mA
I_{OK}	DC Output Diode Current	At V_O < 0 V		–50	mA
		At V_O > V_{CC}		+50	
I_{OH} / I_{OL}	DC Output Source/Sink Current		–50	+50	mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin			±100	mA
P_D	Power Dissipation	At 400 KHz		0.129	mW
T_{STG}	Storage Temperature Range		–65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		8	kV
		Charged Device Mode, JESD22-C101		2	

Note:
2. I_O absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CCA}, V_{CCB}	Power Supply Operating		1.65	5.50	V
V_{IN}	Input Voltage	A Port	0	5.5	V
		B Port	0	5.5	
		Control Input (OE)	0	V_{CCA}	
Θ_{JA}	Thermal Resistance	8-Lead MicroPak™		279.0	C°/W
		8-Lead Ultrathin MLP		301.5	
T_A	Free Air Operating Temperature		–40	+85	°C

Note:
3. All unused inputs and I/O pins must be held at V_{CCI} or GND.

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Functional Description

Power-Up/Power-Down Sequencing

FXM translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 V, outputs are in a high-impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Note:

4. Alternatively, the OE pin can be hardwired to V_{CCA} to save GPIO pins. If OE is hardwired to V_{CCA}, either V_{CC} can be powered up or down first.

Application Circuit

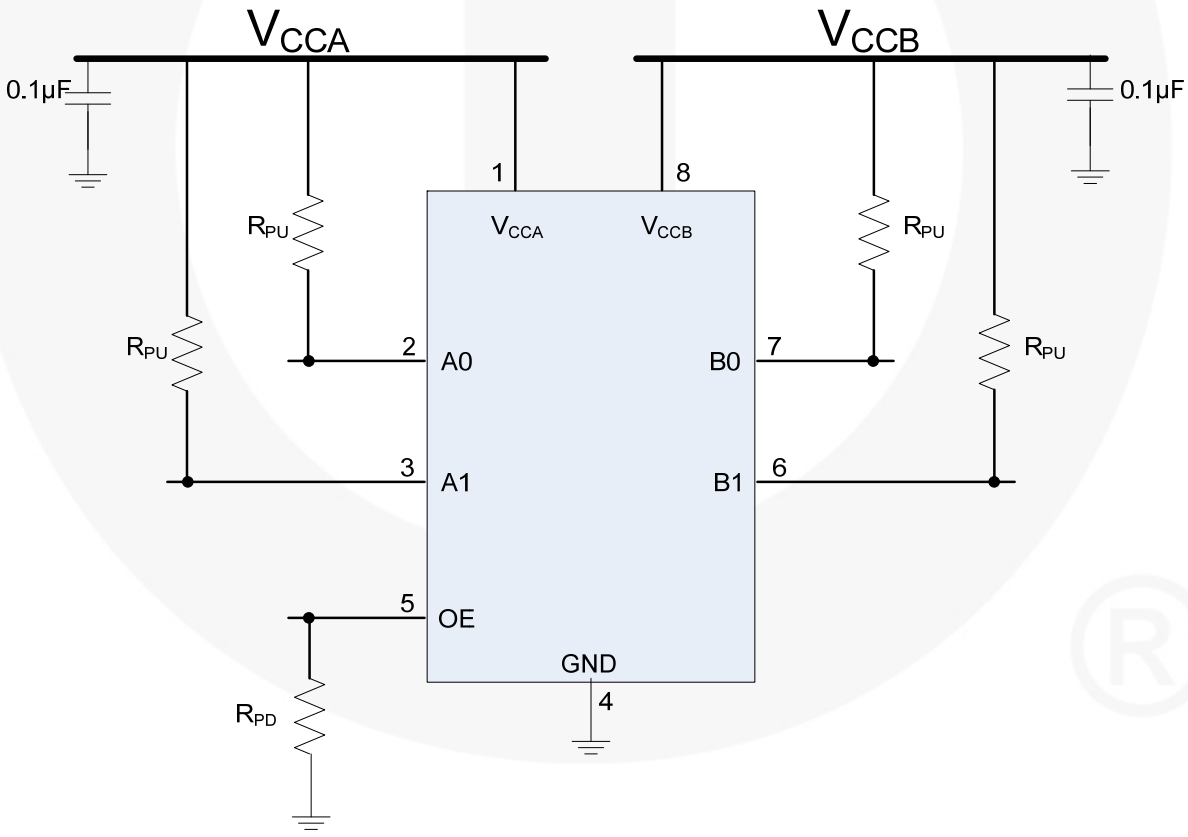

Figure 4. Application Circuit

Application Notes

The FXMA2102 has open-drain I/Os and requires external pull-up resistors on the four data I/O pins, as shown in Figure 4. If a pair of data I/O pins (A_n/B_n) is not used, both pins should be tied to GND (or both to V_{CC}). In this case, pull-down or pull-up resistors are not required. The recommended values for the pull-up resistors (RPU) are 1 KΩ to 10 KΩ; however, depending on the total bus capacitance, the user is free to vary the pull-up resistor value to meet the maximum I^2C edge rate per the I^2C specification (UM10204 rev. 03, June 19, 2007). For example, the maximum edge rate (30% - 70%) during fast mode (400 kbit/s) is 300 ns. If bus capacitance is approaching the maximum 400 pF, lower the RPU value to keep the rise time below 300 ns (Fast Mode). Section 7.1 of the I^2C specification provides an excellent guideline for pull-up resistor sizing.

Theory of Operation

The FXMA2102 is designed for high-performance level shifting and buffer / repeating in an I^2C application. Figure 1 shows that each bi-directional channel contains two series-Npassgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I^2C application where auto-direction is a necessity.

For example, during the following three I^2C protocol events:

- Clock Stretching
- Slave's ACK Bit (9^{th} bit = 0) following a Master's Write Bit (8^{th} bit = 0)
- Clock Synchronization and Multi Master Arbitration

The bus direction needs to change from master to slave to slave to master without the occurrence of an edge. If there is an I^2C translator between the master and slave in these examples, the I^2C translator must change direction when both A and B ports are LOW. The Npassgates can accomplish this task very efficiently because, when both A and B ports are LOW, the Npassgates act as a low resistive short between the two (A and B) ports.

Due to I^2C's open-drain topology, I^2C masters and slaves are not push/pull drivers. Logic LOWs are "pulled down" (I_{sink}), while logic HIGHs are "let go" (3-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant, where R = R_{PU} and C = the bus capacitance. If the FXMA2102 is attached to the master [on the A port] in this example, and there is a slave on the B port, the Npassgates act as a low resistive short between both ports until either of the port's V_{CC}/2 thresholds are reached. After the RC time constant has reached the V_{CC}/2 threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot in Figure 5. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports because both the Npassgates are turned off. If a master or slave device decides to pull SCL or SDA LOW, that device's driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or B port V_{CC}/2 threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

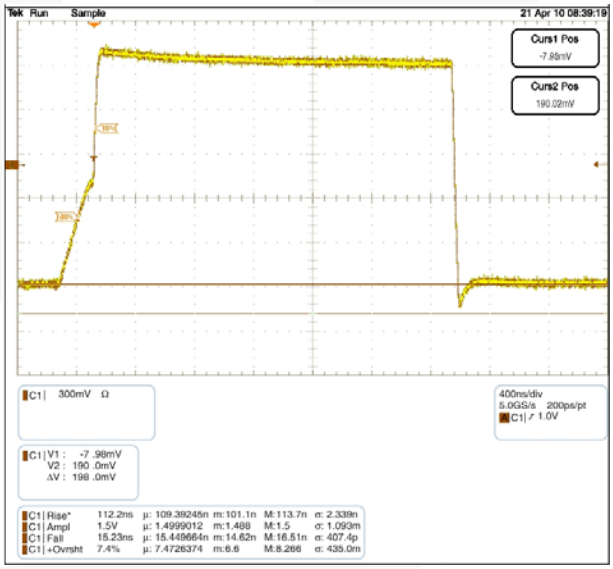

Figure 5. FXMA2102 Waveform C: 600 pF, R_{PU}: 2.2 K

Buffer / Repeater Performance

The FXMA2102 dynamic drivers have enough current sourcing capability to drive a 400 pF capacitive bus. This is beneficial for instances when an I^2C buffer / repeater is required. The I^2C specification stipulates a maximum bus capacitance of 400 pF. If an I^2C segment exceeds 400 pF, an I^2C buffer / repeater is required to split the segment into two segments, each of which is less than 400 pF. Figure 5 is a scope shot of an FXMA2102 driving a lumped load of 600 pF. Notice the (30% - 70%) rise time is only 112 ns (R_{PU} = 2.2 K). This is well below the maximum edge rate of 300 ns. Not only does the FXMA2102 drive 400 pF, but it also provides excellent headroom below the I^2C specification maximum edge rate of 300 ns.

V_{OL} vs. I_{OL}

The I^2C specification mandates a maximum V_{IL} (I_{OL} of 3 mA) of V_{CC} • 0.3 and a maximum V_{OL} of 0.4 V. If there is a master on the A port of an I^2C translator with a V_{CC} of 1.65 V and a slave on the I^2C translator B port with a V_{CC} of 3.3 V, the maximum V_{IL} of the master is (1.65 V x 0.3) 495 mV. The slave could legally transmit a valid logic LOW of 0.4 V to the master.

If the I^2C translator's channel resistance is too high, the voltage drop across the translator could present a V_{IL} to the master greater than 495 mV. To complicate matters, the I^2C specification states that 6 mA of I_{OL} is recommended for bus capacitances approaching 400 pF. More I_{OL} increases the voltage drop across the I^2C translator. The I^2C application benefits when I^2C translators exhibit low V_{OL} performance. Figure 6 depicts typical FXMA2102 V_{OL} performance vs. the competition, given a 0.4 V V_{IL}.

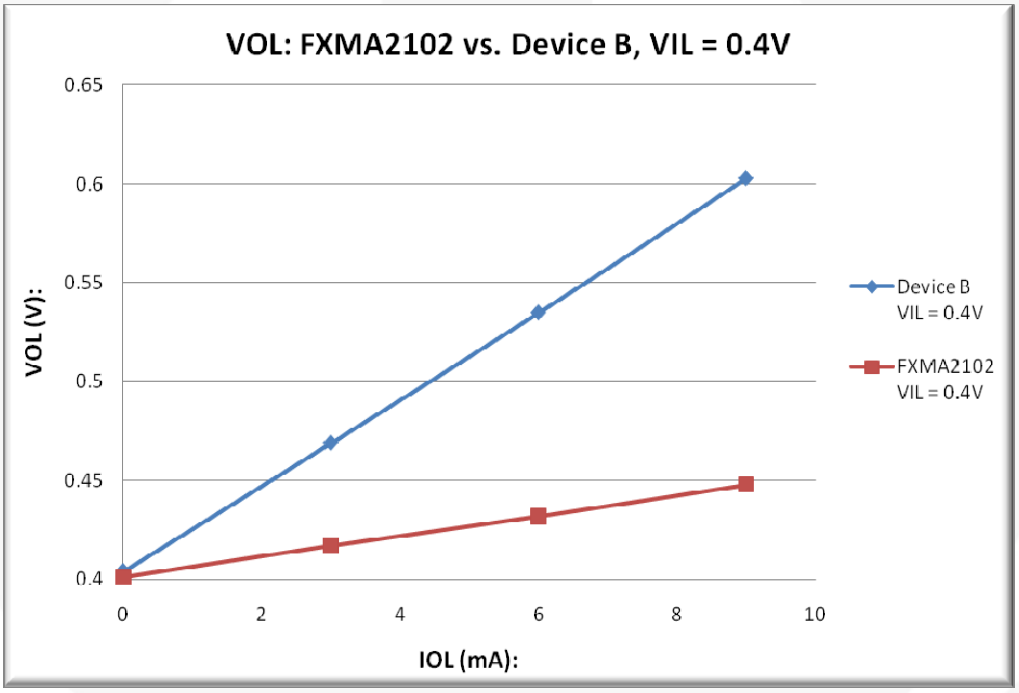

Figure 6. V_{OL} vs. I_{OL}

I²C-Bus® Isolation

The FXMA2102 supports I²C-Bus isolation for the following conditions:

- Bus isolation if bus clear
- Bus isolation if either V_{CC} goes to ground

Bus Clear

Because the I²C specification defines the minimum SCL frequency of DC, the SCL signal can be held LOW forever; however, this condition shuts down the I²C bus. The I²C specification refers to this condition as “Bus Clear”. In Figure 7, if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate, because the FXMA2102 passes the SCL stuck-LOW condition from slave #2 to slave #1 as well as the master. However, if the OE pin is pulled LOW (disabled), both ports (A and B) are 3-stated. This results in the FXMA2102 isolating slave #2 from the master and slave #1, allowing full communication between the master and slave #1.

Either V_{CC} to GND

If slave #2 is a camera that is suddenly removed from the I²C bus, resulting in V_{CCB} transitioning from a valid V_{CC} (1.65 V – 5.5 V) to 0 V, the FXMA2102 automatically forces SCL and SDA on both its A and B ports into 3-state. Once V_{CCB} has reached 0V, full I²C communication between the master and slave #1 remains undisturbed.

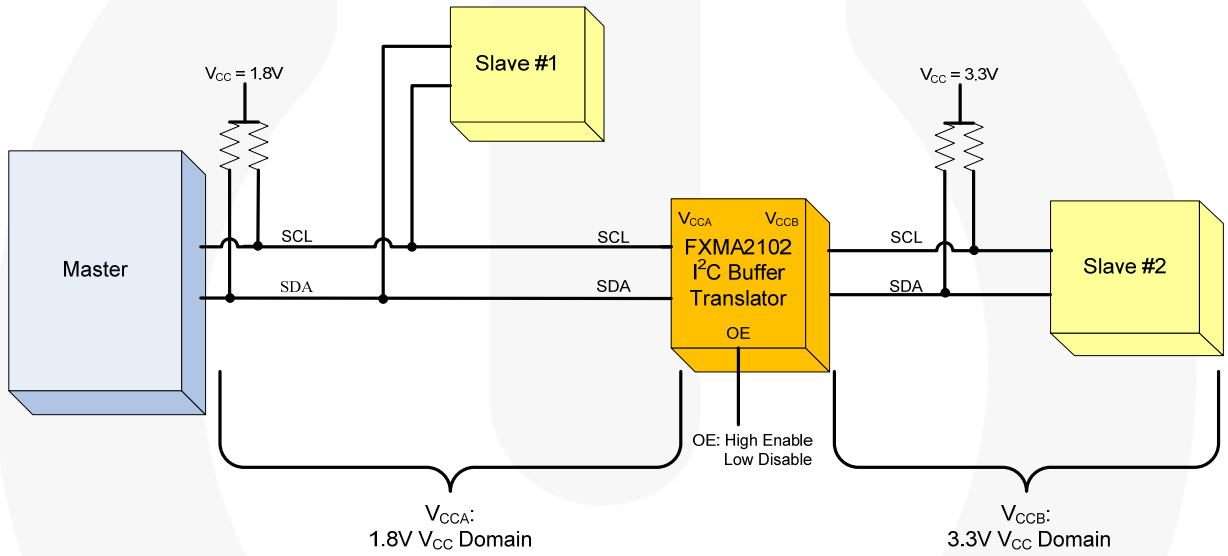

Figure 7. Bus Isolation

DC Electrical Characteristics

T_A = –40°C to +85°C.

Symbol	Parameter	Condition		V_{CCA} (V)	V_{CCB} (V)	Min.	Max.	Unit
V_{IHA}	High Level Input Voltage A	Data Inputs A_n		1.65–5.50	1.65–5.50	V_{CCA} – 0.4		V
		Control Input OE		1.65–5.50	1.65–5.50	0.7 x V_{CCA}		
V_{IHB}	High Level Input Voltage B	Data Inputs B_n		1.65–5.50	1.65–5.50	V_{CCB} – 0.4		V
V_{ILA}	Low Level Input Voltage A	Data Inputs A_n		1.65–5.50	1.65–5.50		0.4	V
		Control Input OE		1.65–5.50	1.65–5.50		0.3 x V_{CCA}	
V_{ILB}	Low Level Input Voltage B	Data Inputs B_n		1.65–5.50	1.65–5.50		0.4	V
V_{OL}	Low Level Output Voltage	V_{IL} = 0.15 V		1.65–5.50	1.65–5.50		0.4	V
		I_{OL} = 6 mA						
I_L	Input Leakage Current	Control Input OE, V_{IN} = V_{CCA} or GND		1.65–5.50	1.65–5.50		±1.0	µA
I_{OFF}	Power Off Leakage Current	A_n	V_{IN} or V_O = 0 V to 5.5 V	0	5.50		±2.0	µA
		B_n	V_{IN} or V_O = 0 V to 5.5 V	5.50	0		±2.0	
I_{OZ}	3-State Output Leakage[6]	A_n, B_n	V_O = 0 V to 5.5 V, OE = V_{IL}	5.50	5.50		±2.0	µA
		A_n	V_O = 0 V to 5.5 V, OE = Don't Care	5.50	0		±2.0	
		B_n	V_O = 0 V to 5.5 V, OE = Don't Care	0	5.50		±2.0	
$I_{CCA}/_B$	Quiescent Supply Current[7,8]	V_{IN} = V_{CCI} or GND, I_O = 0		1.65–5.50	1.65–5.50		5.0	µA
I_{CCZ}	Quiescent Supply Current[7]	V_{IN} = V_{CCI} or GND, I_O = 0, OE = V_{IL}		1.65–5.50	1.65–5.50		5.0	µA
I_{CCA}	Quiescent Supply Current[6]	V_{IN} = 5.5 V or GND, I_O = 0, OE = Don't Care, B_n to A_n		0	1.65–5.50		–2.0	µA
				1.65–5.50	0		2.0	
I_{CCB}	Quiescent Supply Current[6]	V_{IN} = 5.5 V or GND, I_O = 0, OE = Don't Care, A_n to B_n		1.65–5.50	0		–2.0	µA
				0	1.65–5.50		2.0	

Notes:

5. This table contains the output voltage for static conditions. Dynamic drive specifications are given in Dynamic Output Electrical Characteristics.
6. "Don't Care" indicates any valid logic level.
7. V_{CCI} is the V_{CC} associated with the input side.
8. Reflects current per supply, V_{CCA} or V_{CCB}.

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Dynamic Output Electrical Characteristics

Output Rise / Fall Time

Output load: C_L = 50 pF, R_{PU} = 2.2 kΩ, push / pull driver, and T_A = -40°C to +85°C.

Symbol	Parameter	V_{CCO}[10]				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Typ.	Typ.	Typ.	Typ.	
t_{rise}	Output Rise Time; A Port, B Port[11]	3	4	5	7	ns
t_{fall}	Output Fall Time; A Port, B Port[12]	1	1	1	1	ns

Notes:

9. Output rise and fall times guaranteed by design simulation and characterization; not production tested.
10. V_{CCO} is the V_{CC} associated with the output side.
11. *See Figure 12*.
12. *See Figure 13*.

Maximum Data Rate[13]

Output load: C_L = 50 pF, R_{PU} = 2.2 kΩ, push / pull driver, and T_A = -40°C to +85°C.

V_{CCA}	Direction	V_{CCB}				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Min.	Min.	Min.	Min.	
4.5 V to 5.5 V	A to B	37	26	19	10	MHz
	B to A	37	36	35	32	
3.0 V to 3.6 V	A to B	36	25	18	10	MHz
	B to A	25	25	25	24	
2.3 V to 2.7 V	A to B	35	25	18	10	MHz
	B to A	18	18	18	17	
1.65 V to 1.95 V	A to B	32	24	17	10	MHz
	B to A	10	10	10	10	

Note:

13. F-toggle guaranteed by design simulation; not production tested.

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AC Characteristics

Output Load: C_L = 50 pF, R_{PU} = 2.2 kΩ, and T_A = -40°C to +85°C.

Symbol	Parameter	V_{CCB}								Unit
		4.5 to 5.5 V		3.0 to 3.6 V		2.3 to 2.7 V		1.65 to 1.95 V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
V_{CCA} = 4.5 to 5.5 V										
t_{PLH}	A to B	1	3	1	3	1	3	1	3	ns
	B to A	1	3	2	4	3	5	4	7	
t_{PHL}	A to B	2	4	3	5	4	6	5	7	ns
	B to A	2	4	2	5	2	6	5	7	
t_{PZL}	OE to A	4	5	6	10	5	9	7	15	ns
	OE to B	3	5	4	7	5	8	10	15	
t_{PLZ}	OE to A	65	100	65	105	65	105	65	105	ns
	OE to B	5	9	6	10	7	12	9	16	
t_{skew}	A Port, B Port(14)	0.50	1.50	0.50	1.00	0.50	1.00	0.50	1.00	ns
V_{CCA} = 3.0 to 3.6 V										
t_{PLH}	A to B	2.0	5.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	B to A	1.5	3.0	1.5	4.0	2.0	6.0	3.0	9.0	
t_{PHL}	A to B	2.0	4.0	2.0	4.0	2.0	5.0	3.0	5.0	ns
	B to A	2.0	4.0	2.0	4.0	2.0	5.0	3.0	5.0	
t_{PZL}	OE to A	4.0	8.0	5.0	9.0	6.0	11.0	7.0	15.0	ns
	OE to B	4.0	8.0	6.0	9.0	8.0	11.0	10.0	14.0	
t_{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	5	10	4	8	5	10	9	15	
t_{skew}	A Port, B Port(14)	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
V_{CCA} = 2.3 to 2.7 V										
t_{PLH}	A to B	2.5	5.0	2.5	5.0	2.0	4.0	1.0	3.0	ns
	B to A	1.5	3.0	2.0	4.0	3.0	6.0	5.0	10.0	
t_{PHL}	A to B	2.0	5.0	2.0	5.0	2.0	5.0	3.0	6.0	ns
	B to A	2.0	5.0	2.0	5.0	2.0	5.0	3.0	6.0	
t_{PZL}	OE to A	5.0	10.0	5.0	10.0	6.0	12.0	9.0	18.0	ns
	OE to B	4.0	8.0	4.5	9.0	5.0	10.0	9.0	18.0	
t_{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	65	110	65	110	65	115	12	25	
t_{skew}	A Port, B Port(14)	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
V_{CCA} = 1.65 to 1.95 V										
t_{PLH}	A to B	4	7	4	7	5	8	5	10	ns
	B to A	1.0	2.0	1.0	2.0	1.5	3.0	5.0	10.0	
t_{PHL}	A to B	5	8	3	7	3	7	3	7	ns
	B to A	4	8	3	7	3	7	3	7	
t_{PZL}	OE to A	11	15	11	14	14	28	14	23	ns
	OE to B	6	14	6	12	6	12	9	16	
t_{PLZ}	OE to A	75	115	75	115	75	115	75	115	ns
	OE to B	75	115	75	115	75	115	75	115	
t_{skew}	A Port, B Port(14)	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns

Note:

14. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) *(see Figure 15)*. Skew is guaranteed, but not tested.

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Capacitance

T_A = +25°C.

Symbol	Parameter	Condition	Typ.	Unit
C_{IN}	Input Capacitance Control Pin (OE)	$V_{CCA} = V_{CCB}$ = GND	2.2	pF
$C_{I/O}$	Input/Output Capacitance, A_n, B_n	$V_{CCA} = V_{CCB}$ = 5.0 V, OE = GND, VA = VB = 5.0 V	13.0	pF
C_{pd}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB}$ = 5.0 V, V_{IN} = 0 V or V_{CC}, f = 400 KHz	13.5	pF

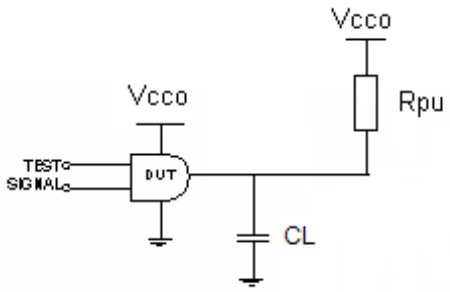

Figure 8. AC Test Circuit

Table 1. Propagation Delay Table

Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	V_{CCA}
t_{PZL} (OE to A_n, B_n)	0 V	LOW to HIGH Switch
t_{PLZ} (OE to A_n, B_n)	0 V	HIGH to LOW Switch

Table 2. AC Load Table

V_{CCO}	C_L	R_L
1.8 ± 0.15 V	50 pF	2.2 kΩ
2.5 ± 0.2 V	50 pF	2.2 kΩ
3.3 ± 0.3 V	50 pF	2.2 kΩ
5.0 ± 0.5 V	50 pF	2.2 kΩ

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Timing Diagrams

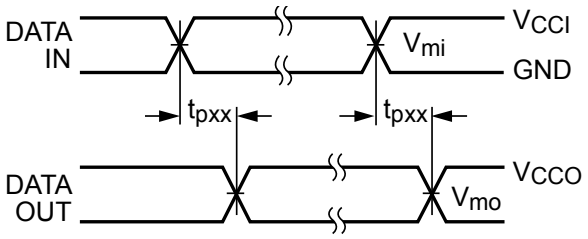


Figure 9. Waveform for Inverting and Non-Inverting Functions[15]

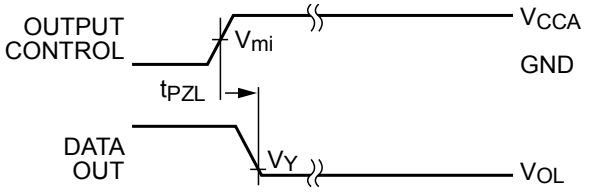


Figure 10. 3-STATE Output Low Enable Time[15]

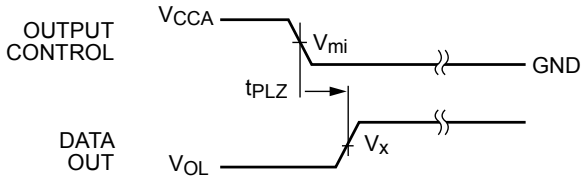


Figure 11. 3-STATE Output High Enable Time[15]

Symbol	V_{CC}
V_{mi}[16]	V_{CCI} / 2
V_{mo}	V_{CCO} / 2
V_X	0.5 x V_{CCO}
V_Y	0.1 x V_{CCO}

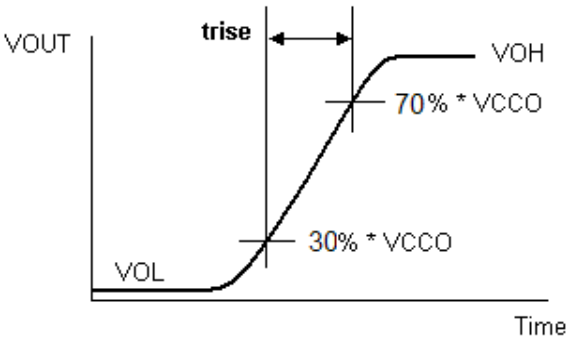


Figure 12. Active Output Rise Time

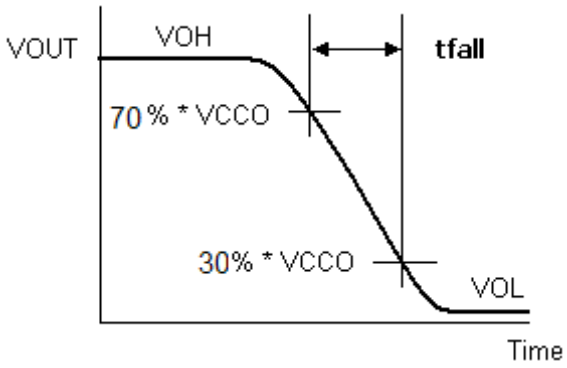


Figure 13. Active Output Fall Time

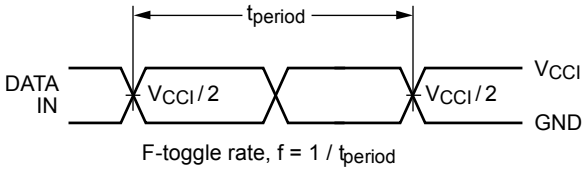
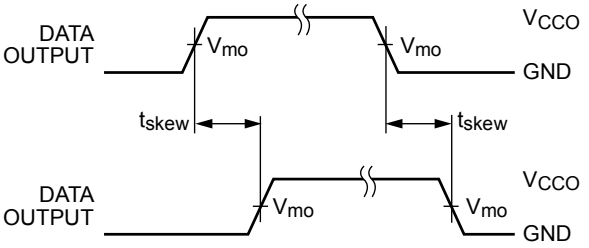


Figure 14. F-Toggle Rate



$t_{skew} = (t_{pHLmax} - t_{pHLmin})$ or $(t_{pLHmax} - t_{pLHmin})$

Figure 15. Output Skew Time

Notes:

15. Input $t_R = t_F$ = 2.0 ns, 10% to 90% at V_{IN} = 1.65 V to 1.95 V;
    Input $t_R = t_F$ = 2.0 ns, 10% to 90% at V_{IN} = 2.3V to 2.7 V;
    Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_{IN} = 3.0 V to 3.6 V only;
    Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_{IN} = 4.5 V to 5.5V only.
16. $V_{CCI} = V_{CCA}$ for control pin OE or $V_{mi} = (V_{CCA} / 2)$.

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8-Lead Ultrathin MLP Product-Specific Dimensions

Symbol from JEDEC MO-220	Description	NOM Value
A	Overall Height	0.55
A1	PKG Standoff	0.012
A3	Lead Thickness	0.15
b	Lead Width	0.2
D	Body Length (X)	1.4
E	Body Width (Y)	1.2
L	Lead Length	0.3
e	Lead Pitch	0.4

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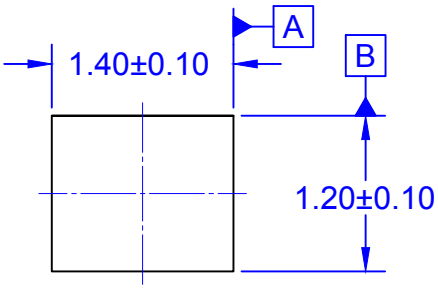
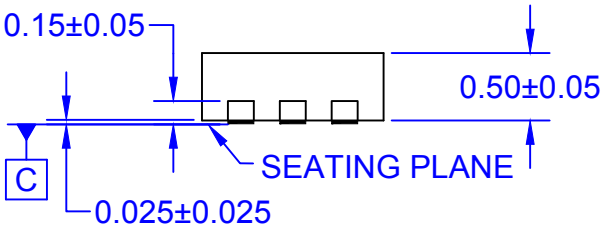
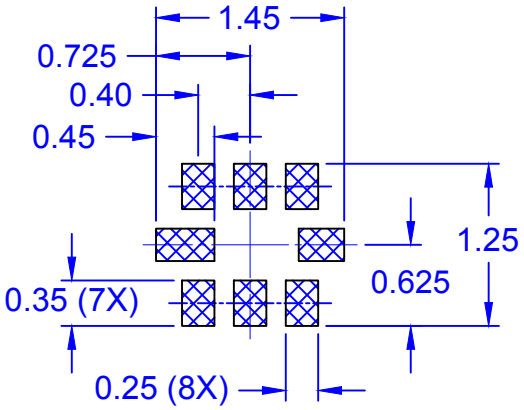


TOP VIEW



SIDE VIEW



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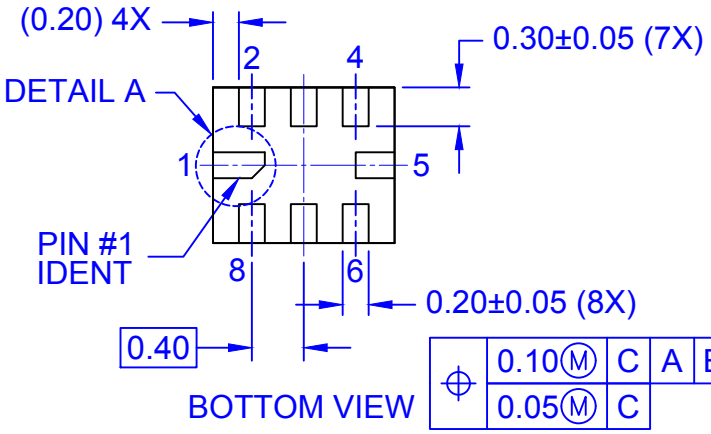
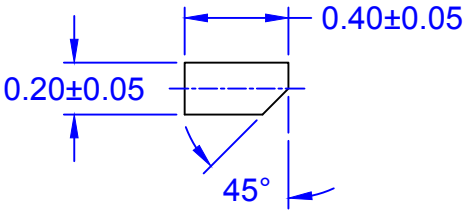


BOTTOM VIEW



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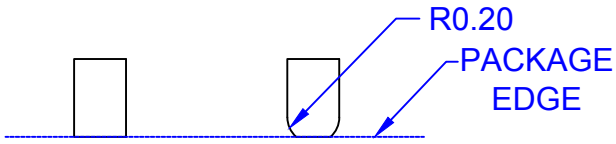

LEAD
OPTION 1
SCALE : 2X

LEAD
OPTION 2
SCALE : 2X

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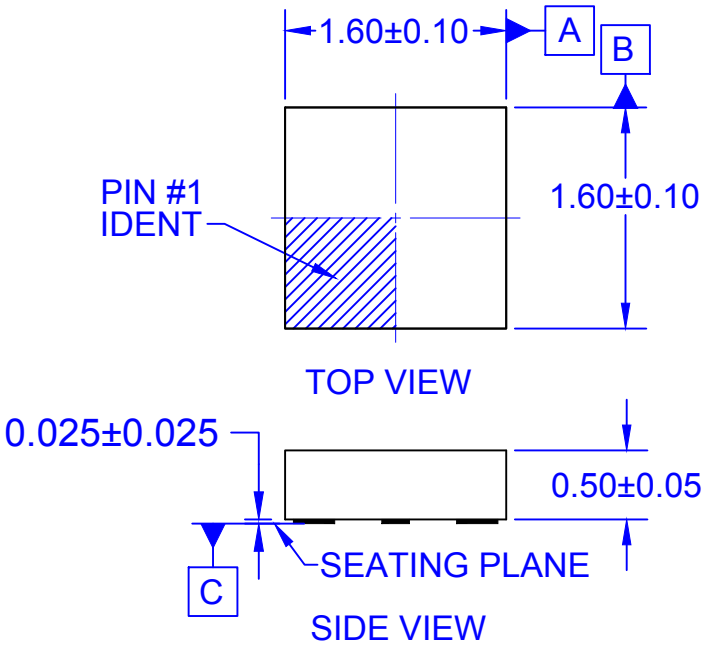

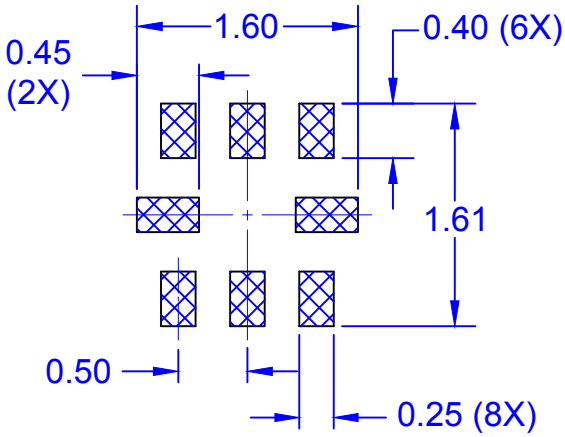

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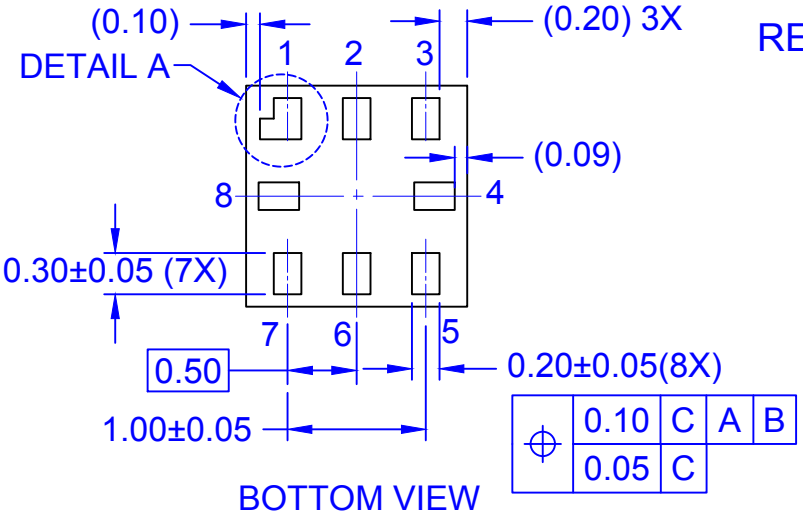

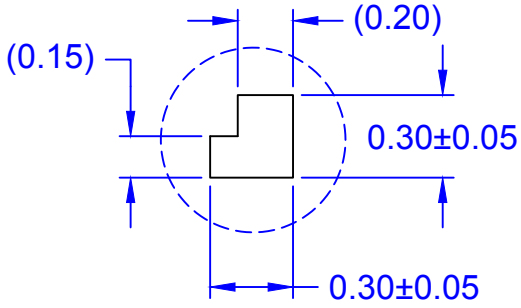

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