DDR Termination Regulator

General Description

The RT9040 is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT9040 possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 20µF of ceramic output capacitance. The RT9040 supports remote sensing functions and all features required to power the DDRI / DDRII / DDRIII and Low Power DDRIII / DDRIV VTT bus termination according to the JEDEC specification. In addition, the RT9040 provides an open drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications .

The RT9040 is available in the thermal efficient WDFN-10L 3x3 package.

Ordering Information

RT9040□□(2)

- Pin 1 Orientation
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

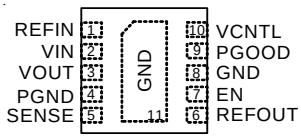
- **V_{IN} Input Voltage Range : 1.1V to 3.5V**
- **V_{CNTL} Input Voltage Range : 2.375V to 5.5V**
- **MLCC Stable**
- **PGOOD to Monitor Output Regulation**
- **±10mA Reference (REFOUT)**
- **Meet DDRI, DDRII JEDEC Spec Supports DDRIII, Low Power DDRIII / DDRIV VTT Application**
- **Soft Start Function UVLO and OCP**
- **UVLO and OCP Protection**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Application

- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV ,Copier/Printer, Set-Top Box

Pin Configurations

(TOP VIEW)



WDFN-10L 3x3

Marking Information

RT9040GQW(2)

G4= : Product Code

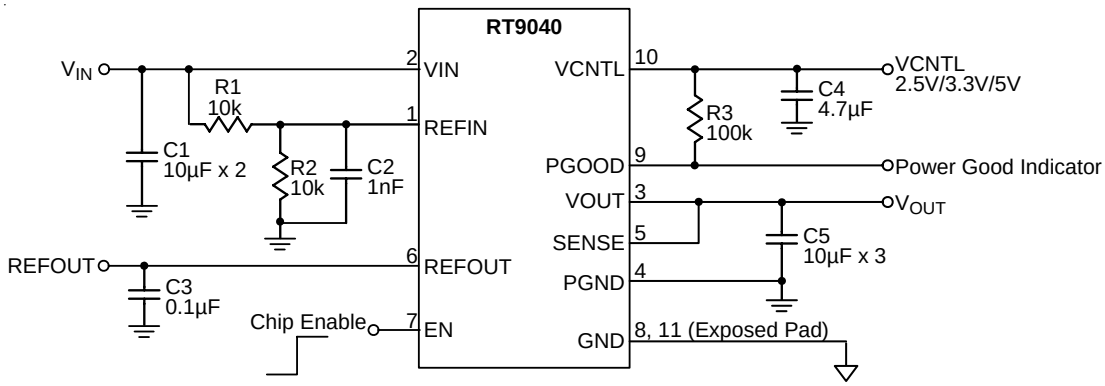
YMDNN : Date Code

RT9040ZQW(2)

G4 : Product Code

YMDNN : Date Code

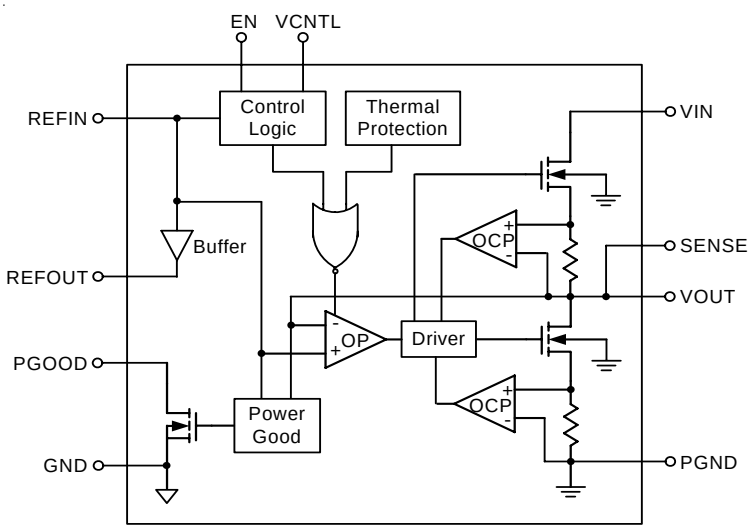
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	REFIN	Reference Input.
2	VIN	Supply Voltage for the LDO.
3	VOUT	Power Output for the LDO.
4	PGND	Power Ground Output for the LDO.
5	SENSE	Voltage Sense Output for the LDO. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	Reference Output. Connect to GND through 0.1uF ceramic capacitor.
7	EN	Chip Enable. For DDR VTT application, connect EN to SLP_S3. For any other application(s), use EN as the ON/OFF function.
8, 11 (Exposed Pad)	GND	Signal Ground. Connect to negative terminal of the output capacitor. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
9	PGOOD	PGOOD Output. Indicates regulation. Connect to an internal open drain N-MOSFET.
10	VCNTL	2.5V, 3.3V or 5V power supply. A ceramic decoupling capacitor with a value between 1µF and 4.7µF is required.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN}, REFIN, VCNTL ---------- 6V
- Enable Voltage, EN ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VCNTL ---------- 2.375V to 5.5V
- Supply Input Voltage, V_{IN} ---------- 1.1V to 3.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 1.8V, V_{EN} = VCNTL = 3.3V, V_{REFIN} = 0.9V, V_{SENSE} = 0.9V, C_{OUT} = 10uF x 3, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCNTL Supply Current	I_{VCNTL}	V_{EN} = 3.3V, No Load	--	0.9	2	mA
VCNTL Shutdown Current	I_{SHDN_VCNTL}	V_{EN} = 0V, V_{REFIN} = 0, No Load	--	65	80	µA
		V_{EN} = 0V, V_{REFIN} > 0.4V, No Load	--	200	500	
VIN Supply Current	I_{VIN}	V_{EN} = 3.3V, No Load	--	--	2	mA
VIN Shutdown Current	I_{SHDN_VIN}	V_{EN} = 0V, No Load	--	0.1	50	µA
Input Current						
REFIN Input Current	I_{REFIN}	V_{EN} = 3.3 V	--	--	1	µA
Output						
Offset Voltage of Output DC Voltage	V_{VOTOL}	VIN = 2.5 V, V_{REFOUT} = 1.25 V (DDRI), I_{OUT} = 0A	--	1.25	--	V
			–10	--	10	mV
		VIN = 1.8 V, V_{REFOUT} = 0.9V (DDRII), I_{OUT} = 0A	--	0.9	--	V
			–10	--	10	mV
		VIN = 1.5 V, V_{REFOUT} = 0.75V (DDRIII), I_{OUT} = 0A	--	0.75	--	V
			–10	--	10	mV
VOUT Load Regulation	ΔV_{LOAD}	–2A < I_{OUT} < 2A	–15	--	15	mV

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Source Current Limit	$I_{LIM\_VOUT\_sr}$	V_{CNTL} = 5V (V_{OUT} in PGOOD window)	3.5	--	5.5	A
VOUT Sink Current Limit	$I_{LIM\_VOUT\_sk}$	V_{CNTL} = 5V (V_{OUT} in PGOOD window)	3.5	--	5.5	A
VOUT Discharge Resistance	$R_{DISCHARGE}$	V_{REFIN} = 0V, V_{OUT} = 0.3V, V_{EN} = 0V	--	18	25	Ω
Power Good Comparator						
VOUT PGOOD Threshold	V_{TH_PGOOD}	PGOOD window lower threshold with respect to REFOUT	–23.5	–20	–17.5	%
		PGOOD Hysteresis	--	5	--	
PGOOD Startup Delay	Tpgdelay1	Startup rising edge, V_{SENSE} within 15% of REFOUT	--	2	--	ms
Output Low Voltage	V_{LOW_PGOOD}	I_{SINK} = 4mA	--	--	0.4	V
PGOOD Bad Delay	Tpgdealy2	V_{SENSE} is outside of the ±20% PGOOD window	--	10	--	μs
Leakage Current	$I_{LEAKAGE\_PGOOD}$	V_{SENSE} = V_{REFIN} (PGOOD high impedance), PGOOD = VCNTL + 0.2 V	--	--	1	μA
REFIN and REFOUT						
REFIN Voltage Range	V_{REFIN}		0.5	--	1.8	V
REFIN Under Voltage Lockout	V_{UVLO_REFIN}	REFIN Rising	360	390	420	mV
		Hysteresis	--	20	--	
REFOUT Voltage Tolerance to VREFIN	V_{TOL_REFOUT}	–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 1.25 V	–15	--	15	mV
		–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.9 V	–15	--	15	
		–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.75V	–15	--	15	
		–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.6V	–15	--	15	
REFOUT Source Current Limit	$I_{LIM\_REFOUT\_sr}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit	$I_{LIM\_REFOUT\_sk}$	V_{REFOUT} = V_{IN}	10	40	--	mA
UVLO / EN Logic Threshold						
UVLO Threshold	V_{UVLO_VCNTL}	Wake up	2.2	2.3	2.375	V
		Hysteresis	--	50	--	mV
High-Level Input Voltage	V_{IN_H}	Enable	1.7	--	--	V
Low-Level Input Voltage	V_{IN_L}	Enable	--	--	0.3	V
Hysteresis Voltage	V_{EN_hys}	Enable	--	0.5	--	V
Logic Input Leakage Current	$I_{LEAKAGE\_EN}$	Enable	–1	--	1	μA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	Shutdown Temperature	--	160	--	°C
		Hysteresis	--	25	--	

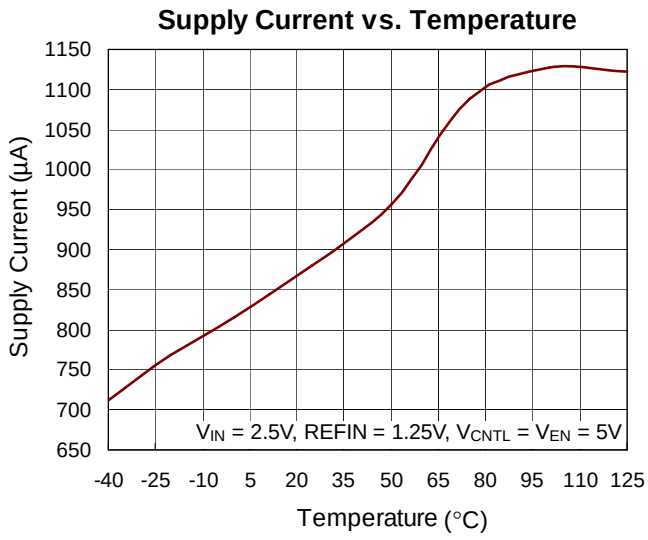
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

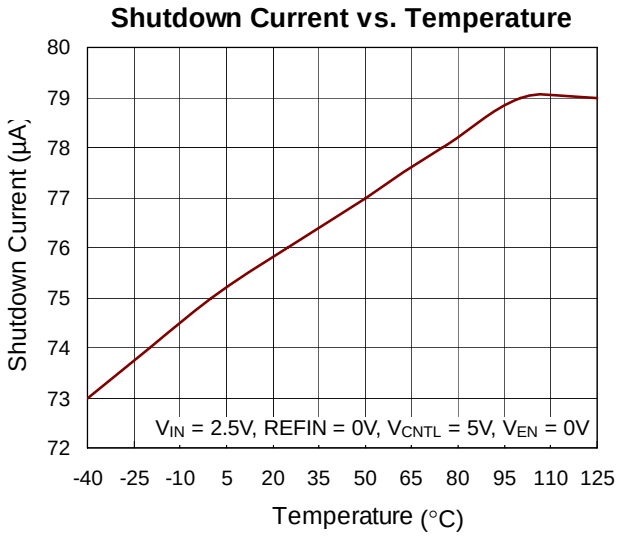
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the WDFN package.

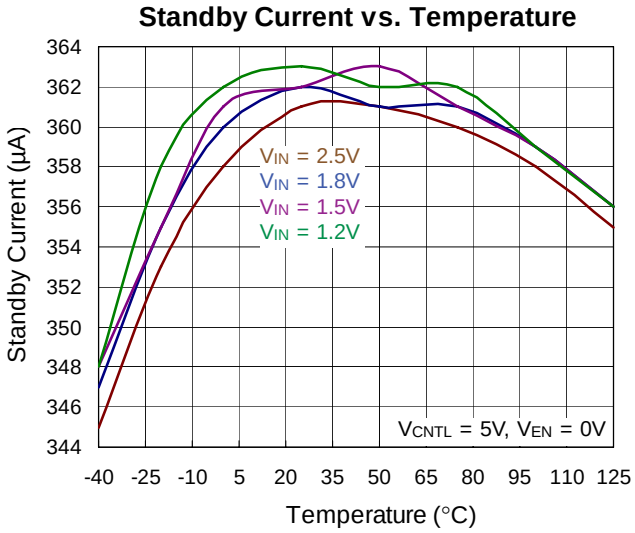
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

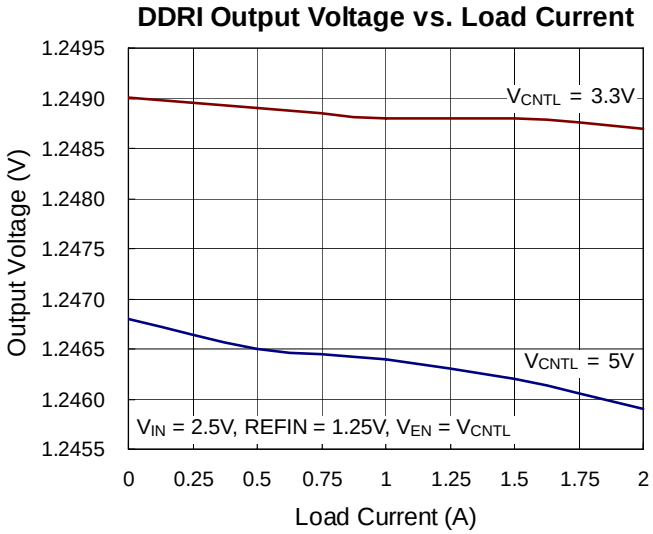
Note 4. The device is not guaranteed to function outside its operating conditions.

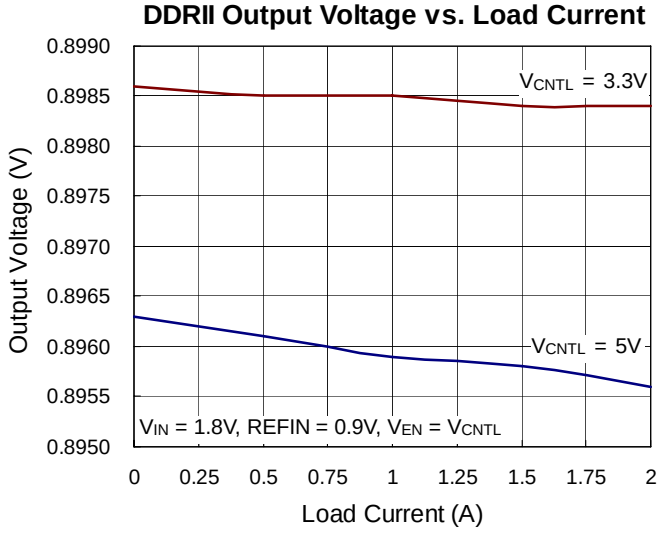
Typical Operating Characteristics

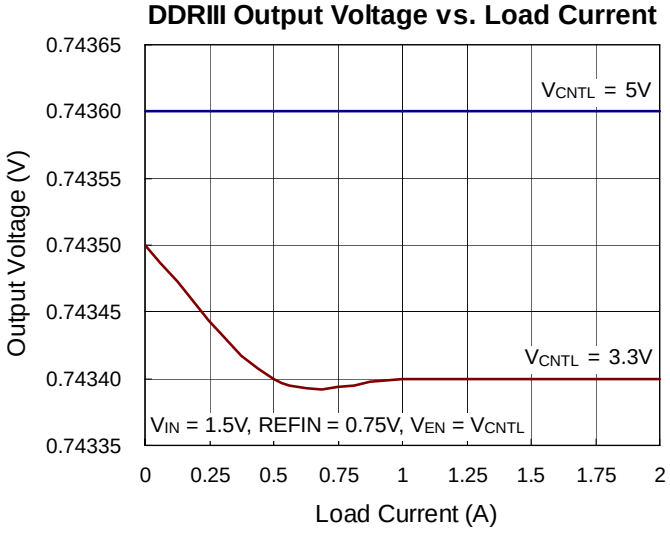




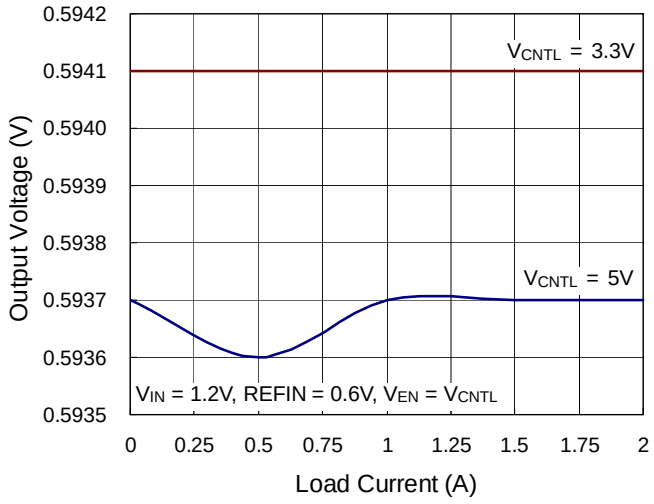




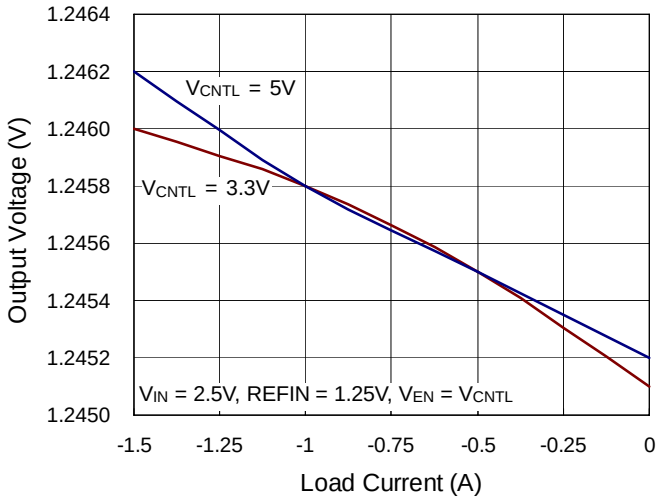




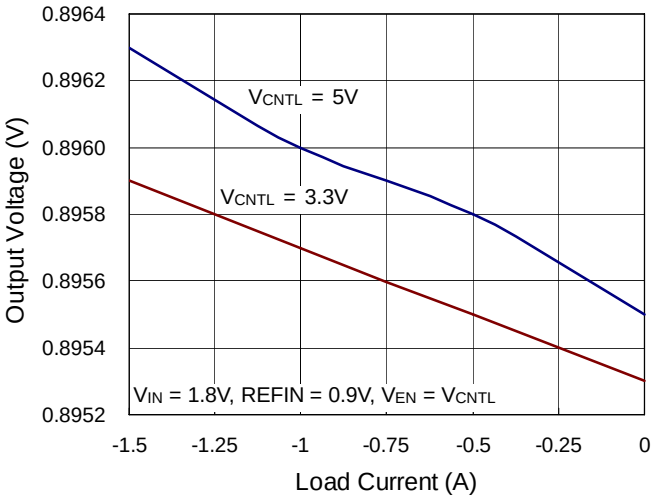
DDRIV Output Voltage vs. Load Current



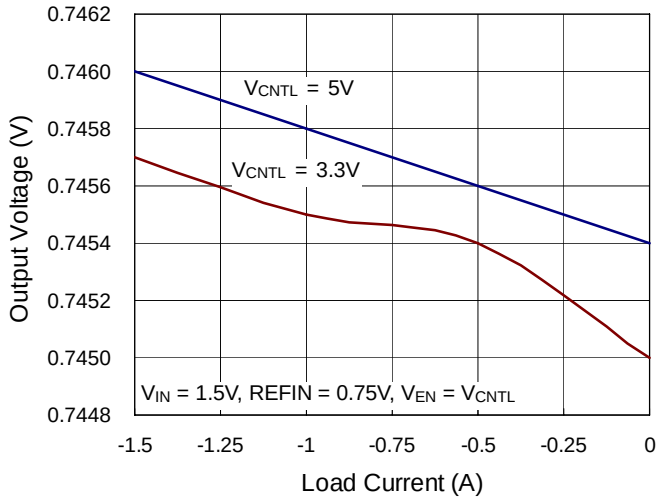
DDRI Output Voltage vs. Load Current



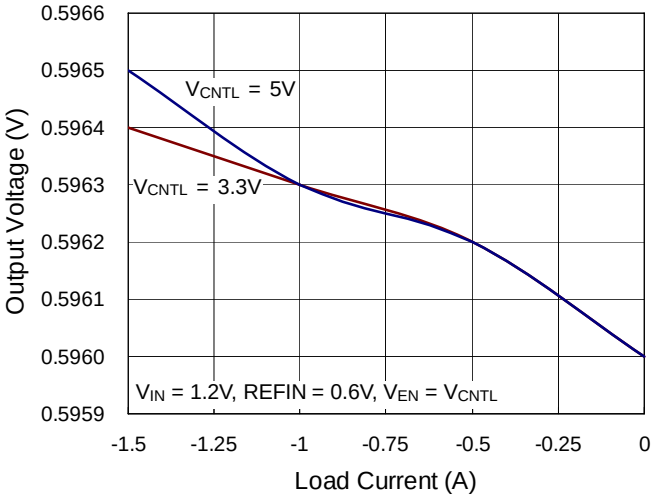
DDRII Output Voltage vs. Load Current



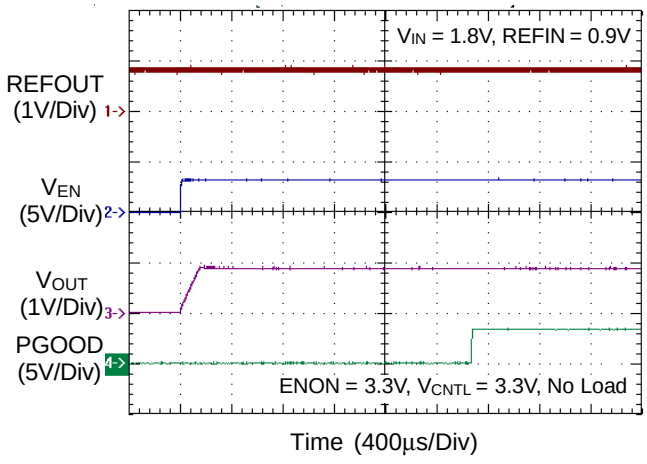
DDRIII Output Voltage vs. Load Current



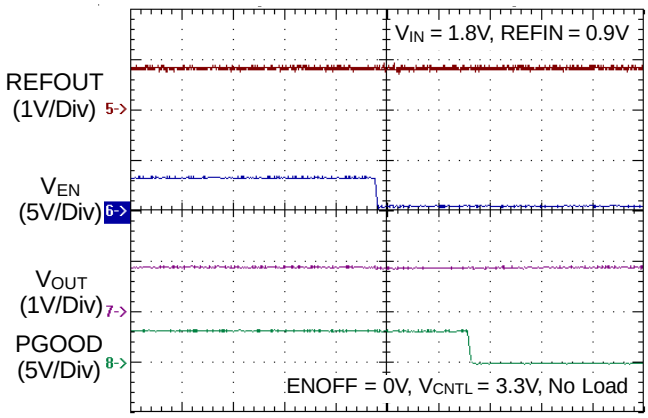
DDRIV Output Voltage vs. Load Current



Power On

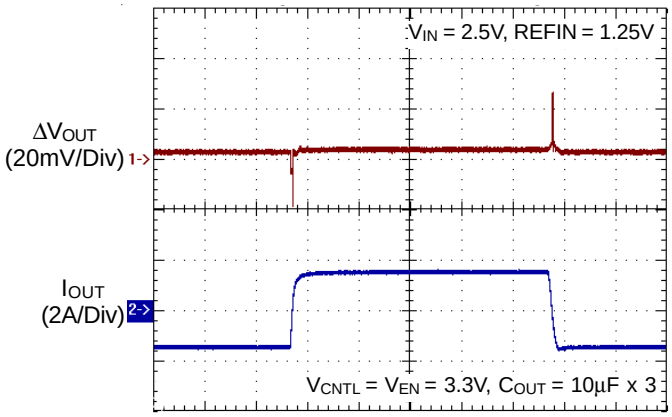


Power Off



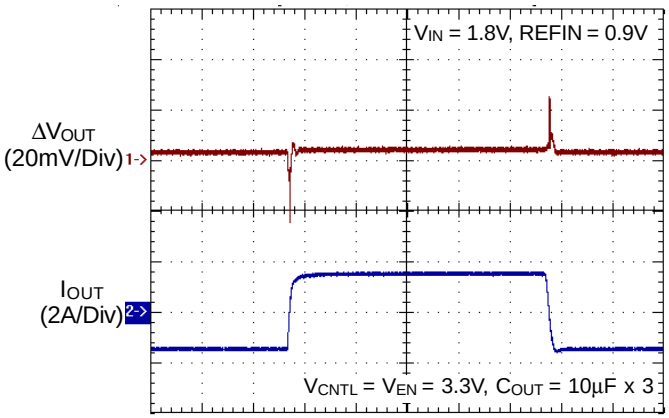
Time (200ns/Div)

1.25V_{OUT} @ ±1.5A Transient Response



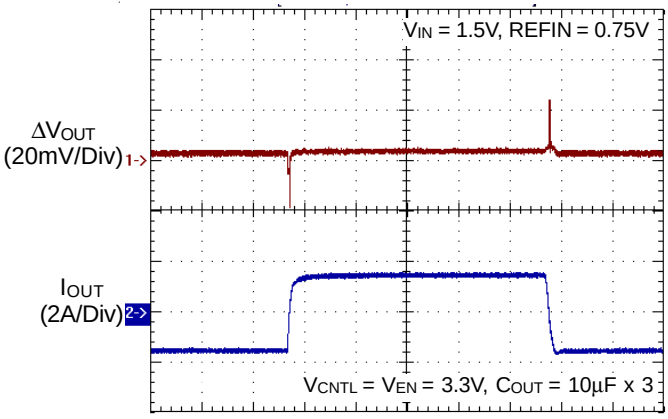
Time (200µs/Div)

0.9V_{OUT} @ ±1.5A Transient Response



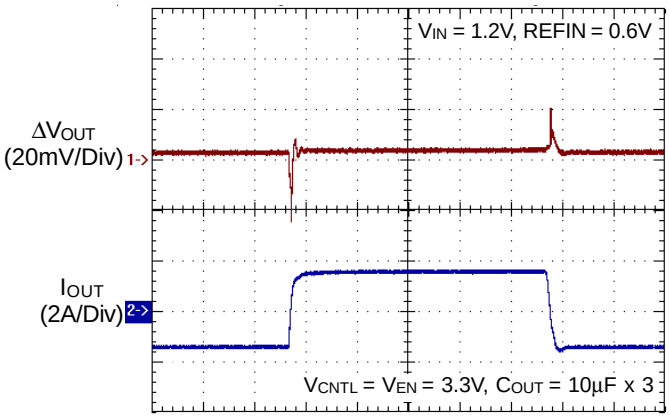
Time (200µs/Div)

0.75V_{OUT} @ ±1.5A Transient Response



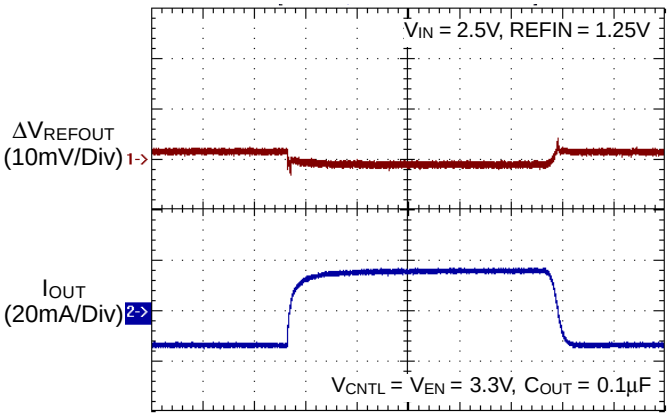
Time (200µs/Div)

0.6V_{OUT} @ ±1.5A Transient Response



Time (200µs/Div)

1.25V_{REFOUT} @ ±15mA Transient Response



Time (400µs/Div)

Application Information

The RT9040 is a sink/source tracking termination regulator.

It is specifically designed for low-cost and low-external component count systems such as notebook PC applications. The RT9040 possesses a high speed operating amplifier that provides fast load transient response and only requires a 10µF ceramic input capacitor and two 10µF ceramic output capacitors.

REFOUT Regulator

REFOUT is a reference output voltage with source/sink current capability up to 10mA. To ensure stable operation, a 0.1µF ceramic capacitor connected between REFOUT and GND is recommended.

Capacitor Selection

To achieve best performance of the RT9040, it is recommended to follow the following descriptions for capacitor selection.

VCNTL Capacitor :

Add a ceramic capacitor 4.7µF placed to VCNTL pin as close as possible to stabilize the supply voltage (2.5V, 3.3V or 5.0V rail) from any parasitic impedance from the supply.

VIN Capacitor :

Good bypassing is recommended from VIN to GND to improve transient response. It is recommended to place two 10µF or greater input capacitor located as close as possible to the IC the capacitor must be placed at less than 0.5 inch from the VIN pin.

VOUT Capacitor :

For stable operation, the total capacitance of the VTT output terminal must be greater than 20µF. The RT9040 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. Three 10µF ceramic capacitors are used in the typical application circuit. The output capacitor should be located near the VOUT pin as close as possible.

Operation State Setting

The EN pin could be connected to SLP_S3 signal for DDR VTT application. Both VOUT and REFOUT are turned on at normal state(EN=High, REFIN >0.39V). In standby state(EN=Low, REFIN >0.39V), REFOUT voltage will be kept alive to discharge VOUT voltage via internal circuit and left VOUT high impedance. When EN=Low and REFIN <0.39V, the RT9040 enter shutdown state, both VOUT and REFOUT will be turned off and discharged to ground via internal MOSFETs. Table 1 summarizes the above-mentioned operation state setting, and figure 1 shows a typical start up and shutdown timing diagram.

Table1. Operation State Settling

STATE	EN	REFIN	VOUT	REFOUT
Normal	High	> 0.39V	ON	ON
Standby	Low	> 0.39V	OFF	ON
Shutdown	Low	< 0.39V	OFF	OFF

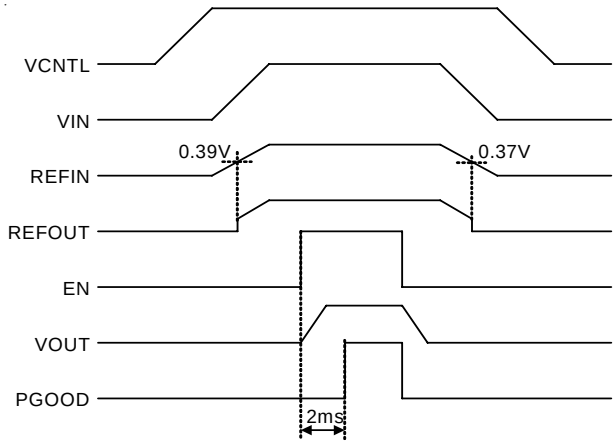


Figure 1. Typical Start Up and Shutdown Timing Diagram

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9040, where $T_{J(MAX)}$ is 125°C and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-10L 3X3 packages, the thermal resistance θ_{JA} is 70°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (70°C/W) = 1.429W for WDFN-10L 3X3 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9040 packages, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

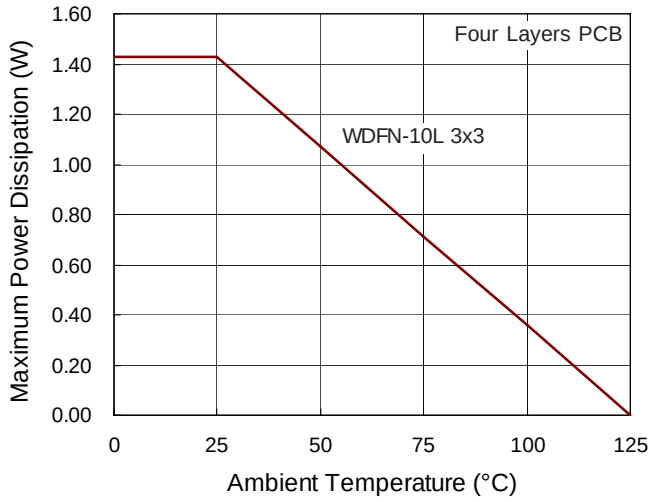
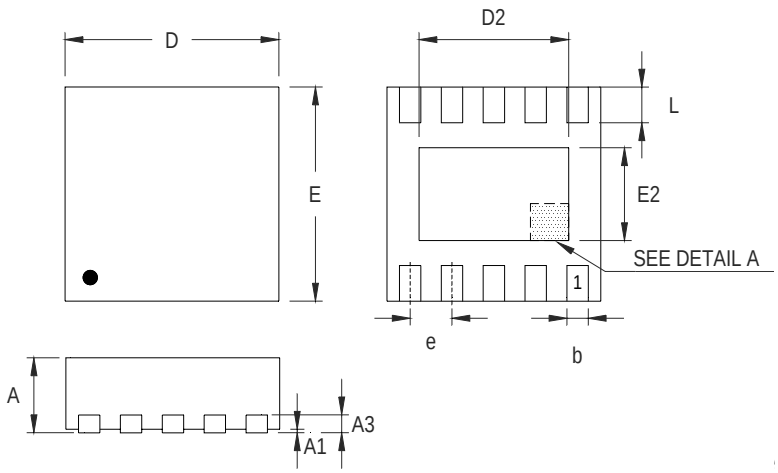
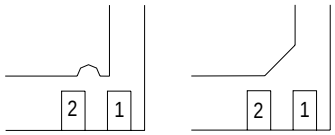


Figure 2. Derating Curves for RT9040 Packages

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com