

Datasheet

V850ES/FF3-L

32-bit Single-Chip Microcontroller

Hardware

μPD70F3615(A)

μPD70F3615(A1)

μPD70F3615(A2)

μPD70F3616(A)

μPD70F3616(A1)

μPD70F3616(A2)

μPD70F3617(A)

μPD70F3617(A1)

μPD70F3617(A2)

μPD70F3618(A)

μPD70F3618(A1)

μPD70F3618(A2)

μPD70F3619(A)

μPD70F3619(A1)

μPD70F3619(A2)

Notes for CMOS Devices

1. Precaution against ESD for semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. Handling of unused input pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. Status before initialization of MOS devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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For further information please contact:

NEC Electronics Corporation

1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668, Japan
Tel: 044 4355111
<http://www.necel.com/>

[America]

NEC Electronics America, Inc.

2880 Scott Blvd.
Santa Clara, CA 95050-2554, I
U.S.A.
Tel: 408 5886000
<http://www.am.necel.com/>

[Europe]

NEC Electronics (Europe) GmbH

Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211 6503-0
<http://www.eu.necel.com/>

United Kingdom Branch

Cygnus House, Sunrise Parkway
Linford Wood
Milton Keynes, MK14 6NP, U.K.
Tel: 01908 691133

Succursale Française

9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01 30675800

Tyskland Filial

Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 6387200

Filiale Italiana

Via Fabio Filzi, 25A
20124 Milano, Italy
Tel: 02 667541

Branch The Netherlands

Steijgerweg 6
5616 HS Eindhoven,
The Netherlands
Tel: 040 2654010

[Asia & Oceania]

NEC Electronics (China) Co., Ltd

7th Floor, Quantum Plaza, No. 27
ZhiChunLu Haidian District,
Beijing 100083, P.R.China
Tel: 010 82351155
<http://www.cn.necel.com/>

NEC Electronics Shanghai Ltd.

Room 2511-2512, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area,
Shanghai 200120, P.R. China
Tel: 021 5888 5400
<http://www.cn.necel.com/>

NEC Electronics Hong Kong Ltd.

Unit 1601-1613, 16/F., Tower 2
Grand Century Place
193 Prince Edward Road West,
Mongkok, Kowloon, Hong Kong
Tel: 2886 9318
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NEC Electronics Taiwan Ltd.

7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R.O.C.
Tel: 02 8175-9600

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238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
<http://www.sg.necel.com/>

NEC Electronics Korea Ltd.

11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku, Seoul,
135-080, Korea
Tel: 02-558-3737
<http://www.kr.necel.com/>

Table of Contents

| | | |
|-----------|---|-----------|
| 1. | Pin Group Information | 6 |
| 1.1 | Device package information | 6 |
| 1.2 | Pin Groups 1x: Pins supplied by EVDD. | 6 |
| 1.3 | Pin Groups 2x: Pins supplied by EVDD. | 6 |
| 1.4 | Pin Groups 3x: Pins supplied by BVDD. | 7 |
| 1.5 | Pin Groups 4: Pins supplied by AVREF0. | 7 |
| 1.6 | Pin Groups 6: Pins supplied by EVDD. | 7 |
| 1.7 | Pin Groups 7: Pins supplied by VRO. | 7 |
| | | |
| 2. | Electrical Specifications | 9 |
| 2.1 | Absolute Maximum Ratings | 9 |
| 2.2 | Capacities | 10 |
| 2.3 | Operating condition. | 10 |
| 2.4 | Voltage Regulator Characteristics | 11 |
| 2.5 | Clock Generator Circuit. | 11 |
| 2.5.1 | Main System Clock Oscillation Circuit Characteristics | 11 |
| 2.5.2 | Sub System Clock Oscillation Circuit Characteristics | 12 |
| 2.5.3 | Internal-OSC Characteristics | 12 |
| 2.5.4 | PLL Characteristics | 13 |
| 2.6 | DC Characteristics | 14 |
| 2.6.1 | Input/Output Level | 14 |
| 2.6.2 | PIN leakage current | 15 |
| 2.6.3 | Power supply current | 16 |
| 2.6.3.1 | FF3-L μ PD70F3615, μ PD70F3616, μ PD70F3617, μ PD70F3618, μ PD70F3619 | 16 |
| 2.7 | AC Characteristics | 21 |
| 2.7.1 | CLKOUT Output Timing | 21 |
| 2.7.2 | RESET, Interrupt, ADTRG Timing. | 22 |
| 2.7.3 | Key Return Timing | 22 |
| 2.7.4 | Timer Timing | 22 |
| 2.7.5 | CSI Timing | 23 |
| 2.7.6 | UART Timing | 23 |
| 2.7.7 | IIC Timing | 24 |
| 2.7.8 | CAN Timing | 26 |
| 2.8 | A/D Converter | 27 |
| 2.9 | POC | 28 |
| 2.10 | LVI | 29 |
| 2.11 | RAM Retention Flag. | 29 |
| 2.12 | Data Retention Characteristics. | 30 |
| 2.13 | Flash Memory Programming Characteristics | 31 |
| | | |
| 3. | Package | 32 |
| 3.1 | Package Dimension | 32 |
| 3.2 | Product Marking. | 33 |
| 3.2.1 | Marking of pin 1 at a QFP (Quad Flat Package) | 33 |
| 3.2.2 | Identification of Lead-Free Products | 34 |
| | | |
| 4. | Change History | 35 |

1. Pin Group Information

1.1 Device package information

The V850ES/Fx3-L device series comprises several members. An overview with the pin and package information is given in the following table:

| Series Member | # Pins | Device package information |
|--|--------|----------------------------|
| μPD70F3610 μPD70F3611 μPD70F3612 μPD70F3613 μPD70F3614 | 64 | FE3-L |
| μPD70F3615 μPD70F3616 μPD70F3617 μPD70F3618 μPD70F3619 | 80 | FF3-L |
| μPD70F3620 μPD70F3621 μPD70F3622 | 100 | FG3-L |

This document describes the specification for the V850ES/FF3-L.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)

- P04, P30-31, P34; P40, P91, P913-915 (FE3-L)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3-L)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3-L)

1D: (SHMT3)

- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3-L)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3-L)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3-L)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)

- PCM0-1 (FE3-L)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3-L)

2D: (SHMT3)

- PDL0-7 (FE3-L)
- PDL0-11 (FF3-L)

1.4 Pin Groups 3x: Pins supplied by BVDD

3A: (CMOS)

- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FG3-L)

3D: (SHMT3)

- PDL0-13 (FG3-L)

1.5 Pin Groups 4: Pins supplied by AVREF0

4: (CMOS)

- P70-79 (FE3-L)
- P70-711 (FF3-L)
- P70-715 (FG3-L)

1.6 Pin Groups 6: Pins supplied by EVDD

- RESET (SHMT2)
- IC, FLMD0

1.7 Pin Groups 7: Pins supplied by VRO

- X1, X2, XT1, XT2

2. Electrical Specifications

This product has to be used only under the conditions of VDD=EVDD. Operation is not ensured at the time of using this product except this condition.

The operating ambient temperature of each quality grade is as follows:

(A)-Grade: Ta = -40 to +85°C

(A1)-Grade: Ta = -40 to +110°C

(A2)-Grade: Ta = -40 to +125°C

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Conditions | Rating | Unit | | |
|-------------------------------|--------|------------------------|-----------------------------|-----------------------|----|-----|
| Supply voltage | VDD | VDD=EVDD, | -0.5 to +6.5 | V | | |
| | EVDD | VDD=EVDD | -0.5 to +6.5 | | | |
| | AVREF0 | | -0.5 to +6.5 | | | |
| | VSS | VSS=EVSS=AVSS | -0.5 to +0.5 | | | |
| | EVSS | VSS=EVSS=AVSS | -0.5 to +0.5 | | | |
| | AVSS | VSS=EVSS=AVSS | -0.5 to +0.5 | | | |
| Input voltage | VI1 | Pin Group 1x, 2x, 6 | -0.5 to EVDD+0.5 Note1 | V | | |
| | VI3 | Pin Group 7 | -0.5 to VRO+0.5 Note1 | | | |
| Analog input voltage | VIAN | Pin Group 4 | -0.5 to AVREF0+0.5 Note1 | V | | |
| High level output current | IOH | Pin Group 1x, 2x | 1 pin | -4 | mA | |
| | | | Total | (A) | | -50 |
| | | | | (A1) | | -20 |
| | | | | (A2) | | -20 |
| | | Pin Group 4 | 1 pin | -4 | | |
| | | | Total | (A) ^{Note2} | | -20 |
| | | | | (A1) ^{Note2} | | -10 |
| | | | | (A2) ^{Note3} | | -10 |
| Low level output current | IOL | Pin Group 1x, 2x | 1 pin | 4 | mA | |
| | | | Total | (A) | | 50 |
| | | | | (A1) | | 20 |
| | | | | (A2) | | 20 |
| | | Pin Group 4 | 1 pin | 4 | | |
| | | | Total | (A) ^{Note2} | | 20 |
| | | | | (A1) ^{Note2} | | 10 |
| | | | | (A2) ^{Note3} | | 10 |
| Operating ambient temperature | Ta | Normal operating mode | (A) | -40 to +85 | °C | |
| | | Flash programming mode | | | | |
| | | Normal operating mode | (A1) | -40 to +110 | | |
| | | Flash programming mode | | | | |
| | | Normal operating mode | (A2) | -40 to +125 | | |
| | | Flash programming mode | | | | |
| Storage temperature | Tstg | | -40 to +125 | °C | | |

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
 2. Excluding ADC IAREF0 current.
 3. Including ADC IAREF0 current.

2.2 Capacities

(Ta = 25°C, VDD = EVDD = AVREF0 = VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|--------|----------------------------------|------|------|------|------|
| Input/output capacitance | CIO | f=1MHz, Not measured pins is 0V. | | | 10 | pF |

2.3 Operating condition

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Internal System clock frequency (f _{VBLK}) | Supply voltage | Operating Condition |
|--|---|---|
| $4.0 \leq f_{xx} \leq 20\text{MHz}$ Note1 | $3.5\text{V} \leq \text{VDD} \leq 5.5\text{V}$ ^{Note1} | Operation of functions is enabled |
| | $3.3\text{V} \leq \text{VDD} < 3.5\text{V}$ | The following functions are operable: <ul style="list-style-type: none"> • CPU • Flash (including programming) • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI |
| | $3.3\text{V} \leq \text{AVRF0} \leq 5.5\text{V}$ | <ul style="list-style-type: none"> • A/D Converter <ul style="list-style-type: none"> • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0) • Refer to chapter '2.8 A/D Converter' for details. |
| $32\text{kHz} \leq f_{XT} \leq 35\text{kHz}$ (Crystal) | $3.3\text{V} \leq \text{VDD} < 5.5\text{V}$ Note1 | - |
| $12.5\text{kHz} \leq f_{XT} \leq 27.5\text{kHz}$ ^{Note2} (RC) | | - |
| f _{RL} (240kHz Internal-OSC) | $3.3\text{V} \leq \text{VDD} < 5.5\text{V}$ ^{Note1} | - |

Notes: 1. VDD = EVDD

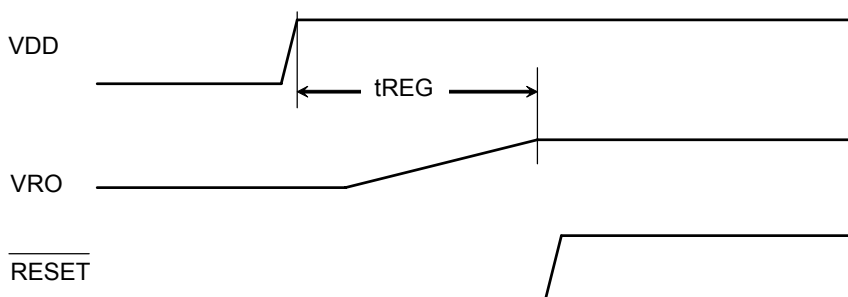
2. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.4 Voltage Regulator Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V))

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|----------------------------------|--|------|------|------|------|
| Input voltage | VDD | | 3.5 | | 5.5 | V |
| | | Limited function see '2.3 Operating condition' | 3.3 | | | V |
| Output voltage | VRO | | | 2.5 | | V |
| Output voltage stabilization time | t _{REG} ^{Note} | After VDD reaches voltage range min. 3.3V To connect C=4.7uF on REGC terminal | | | 1 | ms |

Note: In case of non-POC device, be sure to start VDD in the state of $\overline{\text{RESET}}=\text{VSS}=0\text{V}$.
For POC devices there is no need to control external $\overline{\text{RESET}}$ terminal. For decives with POC function the internal $\overline{\text{RESET}}$ signal will automatically controlled until VRO is stable.



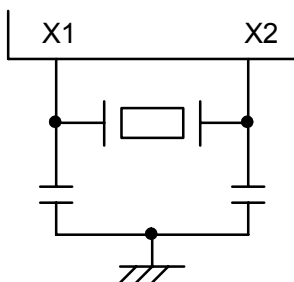
2.5 Clock Generator Circuit

2.5.1 Main System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------|-----------------------|---|------------------|---------------------|-------|------|------|
| Crystal / Ceramic resonator | Refer to figure below | Oscillator frequency (fx) ^{Note1} | | 4 | | 16 | MHz |
| | | Oscillation stabilization time ^{Note2} | After STOP mode | 54 ^{Note4} | Note3 | | μs |
| | | | After IDLE2 mode | 54 ^{Note4} | Note3 | | μs |

- Notes:**
1. Indicates only oscillation circuit characteristics. Refer to '2.7 AC Characteristics' for CPU operation clock.
 2. Time required to stabilize oscillation after VDD reaches oscillator voltage range MIN. 3.3V
 3. Depends on the setting of the oscillation stabilization time select register (OSTS)
 4. Minimum time required to stabilize flash. Time has to be secured by setting the oscillation stabilization time select register (OSTS)



2.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---------------------|---|------------|------|--------|------|------|
| Crystal resonator | Refer to Figure 1 | Oscillator frequency (fxt) ^{Note1} | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time ^{Note2} | | | | 10 | s |

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------|---------------------|---|--|------|------|------|------|
| RC resonator | Refer to Figure 2 | Oscillator frequency ^{Note1,4} | R=390KΩ ±5% ^{Note3} , C=47pF ±10% ^{Note3} | 25 | 40 | 55 | kHz |
| | | Oscillation stabilization time ^{Note2} | | | | 100 | μs |

- Notes:**
1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.
 2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V
 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 4. RC Oscillation frequency is typ. 40kHz. This clock is divided (1/2) internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.



2.5.3 Internal-OSC Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------|-----------------|---------------------|------|------|------|------|
| Output frequency | f _{RL} | 240kHz Internal-OSC | 204 | 240 | 276 | kHz |
| | f _{RH} | 8MHz Internal-OSC | 7.2 | 8.0 | 8.8 | MHz |
| Oscillation stabilization time | | 240kHz Internal-OSC | | 10 | 36 | μs |
| | | 8MHz Internal-OSC | 51 | 92 | 256 | μs |

2.5.4 PLL Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|------------|---|------|------|------|------|
| Input frequency | f_x | | 4 | | 16 | MHz |
| | f_{PLL1} | Note1 | 3 | | 6 | MHz |
| Output frequency | f_{xx} | | 10 | | 20 | MHz |
| Lock time | tPLL | After VDD reaches voltage range min. 3.3V | | | 800 | μs |
| Output period jitter Note2 | tpj | Peak to peak | | | 2.0 | ns |

- Notes:**
1. The input of the PLL (f_{PLL1}) can be set to f_x , $f_x/2$, or $f_x/4$. The divider is set through an option byte in the code flash memory.
 2. Not tested in production.

2.6 DC Characteristics

2.6.1 Input/Output Level

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------|---|---|-------------------|--------------------|------|
| High level input voltage | VIH1 | Pin Group 1B | 0.7·EVDD | | EVDD | V |
| | VIH2 | Pin Group 1D | 0.8·EVDD | | EVDD | V |
| | | Pin Group 2D | 0.8·EVDD | | EVDD | V |
| | VIH3 | Pin Group 2A | 0.7·EVDD | | EVDD | V |
| | VIH4 | Pin Group 4 | 0.7·AVREF0 | | AVREF0 | V |
| Low level input voltage | VIH5 | Pin Group 6 | 0.8·EVDD | | EVDD | V |
| | VIL1 | Pin Group 1B | EVSS | | 0.3·EVDD | V |
| | VIL2 | Pin Group 1D | EVSS | | 0.4·EVDD | V |
| | | Pin Group 2D | EVSS | | 0.4·EVDD | V |
| | VIL3 | Pin Group 2A | EVSS | | 0.3·EVDD | V |
| Input hysteresis | VIL4 | Pin Group 4 | AVSS | | 0.3·AVREF0 | V |
| | VIL5 | Pin Group 6 | EVSS | | 0.2·EVDD | V |
| | VHYS1 | Pin Group 1B | Center point at 0.5·EVDD ^{Note3} | | 0.267·EVDD - 0.51V | V |
| | VHYS2 | Pin Group 1D | Center point at 0.6·EVDD ^{Note3} | | 0.192·EVDD - 0.31V | V |
| | | Pin Group 2D | Center point at 0.6·EVDD ^{Note3} | | 0.192·EVDD - 0.31V | V |
| VHYS5 | Pin Group 6 | Center point at 0.5·EVDD ^{Note3} | | 0.535·EVDD - 0.9V | V | |
| High level output voltage ^{Note2} | VOH1 | Pin Group 1x, 2x | IOH=-1.0mA | EVDD-1.0 | EVDD | V |
| | | | IOH=-100μA | EVDD-0.5 | EVDD | V |
| | VOH3 | Pin Group 4 | IOH=-1.0mA | AVREF0-1.0 | AVREF0 | V |
| | | | IOH=-100μA | AVREF0-0.5 | AVREF0 | V |
| Low level output voltage ^{Note2} | VOL1 | Pin Group 1x, 2x | IOL=1.0mA | 0 | 0.4 | V |
| | | P914, 915 | IOL=3.0mA | | | |
| | VOL3 | Pin Group 4 | IOL=1.0mA | 0 | 0.4 | V |
| Software pull-up resistor | R1 | VI=0V | 10 | 30 | 100 | kΩ |
| Software ^{Note1} pull-down resistor | R2 | VI=VDD | 10 | 30 | 100 | kΩ |

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

- Notes:**
1. $\overline{\text{DRST}}$ terminal only. (Control register is OCDM)
 2. Total IOH/IOL for each power supply line (EVDD and AVREF0).
 - (A-Grade) :max 20mA/-20mA
 - (A1-/A2-Grade): max. 10mA/-10mA
 AVREF0 IOH/IOL current is excluding ADC0 current IAREF0.
 3. Typical value. Not tested and guaranteed

2.6.2 PIN leakage current

(C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | | | Unit | |
|-----------------------------------|--------|------------|------|------|-----------------------------|------|------|------|----|
| | | | | | (A) | (A1) | (A2) | | |
| High level input leakage current | ILIH1 | VI=VDD | | | Analog pins | 0.2 | 0.4 | 0.5 | μA |
| | | | | | Other pins ^{Note1} | 0.5 | 0.8 | 1.0 | |
| Low level input leakage current | ILIL1 | VI=0V | | | Analog pins | -0.2 | -0.4 | -0.5 | |
| | | | | | Other pins ^{Note1} | -0.5 | -0.8 | -1.0 | |
| High level output leakage current | ILOH1 | VO=VDD | | | Analog pins | 0.2 | 0.4 | 0.5 | |
| | | | | | Other pins | 0.5 | 0.8 | 1.0 | |
| Low level output leakage current | ILOL1 | VO=0V | | | Analog pins | -0.2 | -0.4 | -0.5 | |
| | | | | | Other pins | -0.5 | -0.8 | -1.0 | |

Notes: 1. The input leakage current of FLMD0 is as follows:

High level input leakage current :

- (A)-Grade 2.0μA
- (A1)-Grade 4.0μA
- (A2)-Grade 5.0μA

Low level input leakage current:

- (A)-Grade -2.0μA
- (A1)-Grade -4.0μA
- (A2)-Grade 5.0μA

2.6.3 Power supply current

2.6.3.1 FF3-L μ PD70F3615, μ PD70F3616, μ PD70F3617, μ PD70F3618, μ PD70F3619

(a) Absolute values

($T_a = -40$ to $+85^\circ\text{C}$ for (A)-Grade, $T_a = -40$ to $+110^\circ\text{C}$ for (A1)-Grade, $T_a = -40$ to $+125^\circ\text{C}$ for (A2)-Grade,
 $C=4.7\mu\text{F}$, $V_{DD} = EV_{DD} = 3.3$ to 5.5V , $AVREF0 = 3.3$ to 5.5V , $V_{SS} = EV_{SS} = AV_{SS} = 0\text{V}$ ^{Note1})

| Mode | Symbol | Condition | | | TYP. | MAX. | | | Unit |
|-------------------------|--|--|--|---|------|------|------|------|------|
| | | | | | | (A) | (A1) | (A2) | |
| Operating mode Note2 | IDD1 | All peripherals running | Peripheral: f_{xx} PRSI option: 0 | PLL: ON $16\text{MHz} \leq f_{xx} \leq 20\text{MHz}$ $f_{xx}=10\text{MHz}$ $f_x=5\text{MHz}$ | 16 | 24 | | | mA |
| | | | | $f_{xx}=20\text{MHz}$ $f_x=10\text{MHz}$ | 25 | 35 | | | mA |
| | | | | PLL: OFF $4\text{MHz} \leq f_{xx} \leq 16\text{MHz}$ $f_{xx}=8\text{MHz}$ 8MHz Internal-OSC ^{Note3} | 12 | 19 | | | mA |
| | | | | $f_{xx}=16\text{MHz}$ $f_x=16\text{MHz}$ | 20 | 28 | | | mA |
| | | | | PLL: ON $10\text{MHz} \leq f_{xx} \leq 20\text{MHz}$ $f_{xx}=20\text{MHz}$ $f_x=10\text{MHz}$ | 22 | 32 | | | mA |
| | | All peripherals stopped | Peripheral: f_{xx} PRSI option: 0 | PLL: ON $16\text{MHz} \leq f_{xx} \leq 20\text{MHz}$ $f_{xx}=10\text{MHz}$ $f_x=5\text{MHz}$ | 13 | - | | | mA |
| | | | | $f_{xx}=20\text{MHz}$ $f_x=10\text{MHz}$ | 21 | | | | mA |
| | | | | PLL: OFF $4\text{MHz} \leq f_{xx} \leq 16\text{MHz}$ $f_{xx}=8\text{MHz}$ 8MHz Internal-OSC ^{Note3} | 11 | | | | mA |
| | | | | $f_{xx}=16\text{MHz}$ $f_x=16\text{MHz}$ | 18 | | | | mA |
| | | | | PLL: ON $10\text{MHz} \leq f_{xx} \leq 20\text{MHz}$ $f_{xx}=20\text{MHz}$ $f_x=10\text{MHz}$ | 21 | | | | mA |
| All peripherals stopped | Peripheral: $f_{xx}/2$ PRSI option: 1 | PLL: ON $10\text{MHz} \leq f_{xx} \leq 20\text{MHz}$ $f_{xx}=20\text{MHz}$ $f_x=10\text{MHz}$ | 22 | 32 | | | mA | | |

| Mode | Symbol | Condition | | | | TYP. | MAX. | | | Unit | |
|-----------|--------|-------------------------|---|--|---|---|------|------|------|------|----|
| | | | | | | | (A) | (A1) | (A2) | | |
| HALT mode | IDD2 | All peripherals running | Peripheral: f _{xx} PRSI option: 0 | PLL: ON 16MHz ≤ f _{xx} ≤ 20MHz | f _{xx} =10MHz f _x =5MHz | 10 | 15 | | | mA | |
| | | | | | f _{xx} =20MHz f _x =10MHz | 17 | 25 | | | mA | |
| | | | | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz | f _{xx} =8MHz 8MHz Internal-OSC <small>Note3</small> | 7 | 11 | | | mA | |
| | | | | | f _{xx} =16MHz f _x =16MHz | 12 | 18 | | | mA | |
| | | | | Peripheral: f _{xx} /2 PRSI option: 1 | PLL: ON 10MHz ≤ f _{xx} ≤ 20MHz | f _{xx} =20MHz f _x =10MHz | 14 | 21 | | | mA |
| | | | | | | | | | | | |
| | | All peripherals stopped | Peripheral: f _{xx} PRSI option: 0 | PLL: ON 16MHz ≤ f _{xx} ≤ 20MHz | f _{xx} =10MHz f _x =5MHz | 7 | - | | | mA | |
| | | | | | f _{xx} =20MHz f _x =10MHz | 12 | | | | mA | |
| | | | | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz | f _{xx} =8MHz 8MHz Internal-OSC <small>Note3</small> | 5 | | | | mA | |
| | | | | | f _{xx} =16MHz f _x =16MHz | 9 | | | | mA | |
| | | | | Peripheral: f _{xx} /2 PRSI option: 1 | PLL: ON 10MHz ≤ f _{xx} ≤ 20MHz | f _{xx} =20MHz f _x =10MHz | | | | 11 | mA |

| Mode | Symbol | Condition | | | TYP. | MAX. | | | Unit |
|-------------------------------------|-------------------------|--|--|---|------|------|------|------|------|
| | | | | | | (A) | (A1) | (A2) | |
| IDLE1 mode | IDD3 | Peripheral (TAA, UARTD) running | PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7 | f _{xx} =5MHz f _x =5MHz | 1.4 | 2.2 | 2.5 | 2.8 | mA |
| | | | | f _{xx} =12MHz f _x =12MHz | 2.0 | 3.1 | 3.4 | 3.7 | mA |
| | | | | f _{xx} =16MHz f _x =16MHz | 2.4 | 3.6 | 3.9 | 4.2 | mA |
| | | fxx=8MHz, 8MHz Internal-OSC ^{Note3} | | | 1.5 | 2.3 | 2.6 | 2.9 | mA |
| | All peripherals stopped | PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7 | | f _{xx} =5MHz f _x =5MHz | 1.2 | - | | | mA |
| | | | | f _{xx} =12MHz f _x =12MHz | 1.4 | | | | mA |
| | | | | f _{xx} =16MHz f _x =16MHz | 1.6 | | | | mA |
| | | | | fxx=8MHz, 8MHz Internal-OSC ^{Note3} | | | | | 1.1 |
| IDLE2 mode | IDD4 | PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7 | | f _{xx} =5MHz f _x =5MHz | 0.4 | 0.7 | 0.9 | 1.1 | mA |
| | | | | f _{xx} =12MHz f _x =12MHz | 0.7 | 1.0 | 1.2 | 1.5 | mA |
| | | | | f _{xx} =16MHz f _x =16MHz | 0.8 | 1.2 | 1.4 | 1.7 | mA |
| | | | | fxx=8MHz, 8MHz Internal-OSC ^{Note3} | | | 0.2 | 0.5 | 0.7 |
| SUB operating mode ^{Note5} | IDD5 | Crystal resonator (fxt = 32,768kHz) | | | 80 | 400 | - | - | μA |
| | | RC resonator (fxt=20kHz) ^{Note6} | | | 80 | 400 | 600 | 850 | μA |
| | | 240 kHz Internal-OSC (SubOSC stopped) | | | 220 | 1000 | 1200 | 1450 | μA |
| SubIDLE mode ^{Note3,5} | IDD6 | Crystal resonator (fxt = 32,768kHz) | | | 20 | 190 | - | - | μA |
| | | RC resonator (fxt=20kHz) ^{Note6} | | | 40 | 220 | 420 | 670 | μA |
| | | 240kHz Internal-OSC (SubOSC stopped) | | | 25 | 180 | 380 | 630 | μA |
| STOP mode ^{Note3,4} | IDD7 | POC stop | 240kHz Internal-OSC stop | | 7.5 | 80 | 280 | 530 | μA |
| | | | 240kHz Internal-OSC working | | 15.5 | 95 | 295 | 545 | μA |
| | | POC work | 240kHz Internal-OSC stop | | 10.5 | 85 | 285 | 535 | μA |
| | | | 240kHz Internal-OSC working | | 18.5 | 100 | 300 | 550 | μA |

(b) Calculation formulas

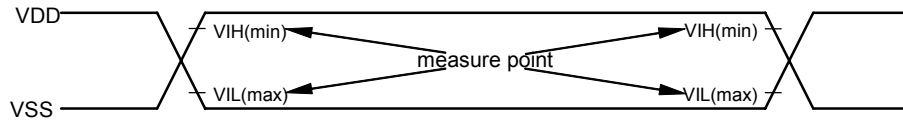
(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V^{Note1)})

| Mode | Symbol | Condition | | TYP. Note8 | MAX. Note8 | | | Unit | |
|-------------------------|--------|--|--|--|------------------------------|------------------------------|------------------------------|------|----|
| | | | | | (A) | (A1) | (A2) | | |
| Operating mode Note2 | IDD1 | All peripherals running | Peripheral: f _{xx} PRSI option: 0 | PLL: ON 16MHz ≤ f _{xx} ≤ 20MHz | 0.93·f _{xx} +6.3 | 1.12·f _{xx} +12.6 | | | mA |
| | | | | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz | 0.93·f _{xx} +4.7 | 1.12·f _{xx} +9.7 | | | mA |
| | | | Peripheral: f _{xx} /2 PRSI option: 1 | PLL: ON 10MHz ≤ f _{xx} ≤ 20MHz | 0.85·f _{xx} +5.2 | 1.03·f _{xx} +11.3 | | | mA |
| | | All peripherals stopped | Peripheral: ff _{xx} - PRSI option: 0 | PLL: ON 16MHz ≤ f _{xx} ≤ 20MHz | 0.78·f _{xx} +5.4 | - | | | mA |
| | | | | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz | 0.80·f _{xx} +4.9 | | | | mA |
| | | | Peripheral: f _{xx} /2 PRSI option: 1 | PLL: ON 10MHz ≤ f _{xx} ≤ 20MHz | 0.76·f _{xx} +5.4 | | | | mA |
| HALT mode | IDD2 | All peripherals running | Peripheral: ff _{xx} - PRSI option: 0 | PLL: ON 16MHz ≤ f _{xx} ≤ 20MHz | 0.70·f _{xx} +3.0 | 0.97·f _{xx} +5.2 | | | mA |
| | | | | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz | 0.65·f _{xx} +1.9 | 0.90·f _{xx} +3.6 | | | mA |
| | | | Peripheral: f _{xx} /2 PRSI option: 1 | PLL: ON 10MHz ≤ f _{xx} ≤ 20MHz | 0.54·f _{xx} +2.8 | 0.63·f _{xx} +8.60 | | | mA |
| | | All peripherals stopped | Peripheral: f _{xx} PRSI option: 0 | PLL: ON 16MHz ≤ f _{xx} ≤ 20MHz | 0.46·f _{xx} +2.8 | - | | | mA |
| | | | | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz | 0.44·f _{xx} +1.6 | | | | mA |
| | | | Peripheral: f _{xx} /2 PRSI option: 1 | PLL: ON 10MHz ≤ f _{xx} ≤ 20MHz | 0.46·f _{xx} +1.8 | | | | mA |
| IDLE1 mode | IDD3 | Peripheral (TAA, UARTD) running | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz | 0.092·f _{xx} +0.90 | 0.128·f _{xx} + 1.52 | 0.128·f _{xx} + 1.82 | 0.128·f _{xx} + 2.12 | mA | |
| | | All peripherals stopped | | 0.035·f _{xx} +1.01 | - | | | mA | |
| IDLE2 mode | IDD4 | PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz Note7 | | 0.037·f _{xx} +0.21 | 0.049·f _{xx} + 0.43 | 0.049·f _{xx} + 0.63 | 0.049·f _{xx} + 0.88 | mA | |

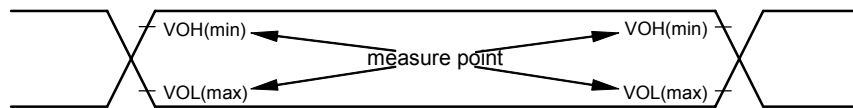
- Notes:**
1. VDD and EVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.
 2. The code flash is in read mode.
When the device is in programming mode (Self-programming mode) the current value (MAX. value) adds by the following value:
 - Self-programming mode:
 - + In case of PLL OFF: $7-(0.33*f_{xx}+0.1)$ [mA]
 - + In case of PLL ON: $7-(0.18*f_{xx}+3.0)$ [mA]
 3. Main OSC is stopped.
 4. Do not use SubOSC.
 5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
 6. RC Oscillation frequency is typ.40kHz. This clock is divided by 1/2 internally.
 7. 8MHz Internal-OSC is stopped
 8. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

2.7 AC Characteristics

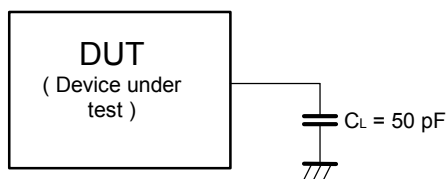
AC test Input measurement points (VDD, AVREF0, EVDD)



AC test output measurement points



Load conditions



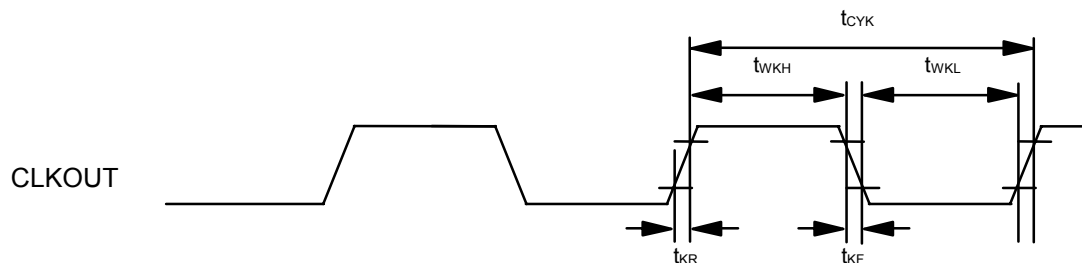
Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

2.7.1 CLKOUT Output Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|------------------|--------|--------------------------|-----------|------|------|
| Output cycle | tCYK | | 50ns | 80μs | |
| High level width | tWKH | VDD = EVDD = 4.0V ~ 5.5V | tCYK/2-13 | | ns |
| | | VDD = EVDD = 3.5V ~ 5.5V | tCYK/2-15 | | |
| Low level width | tWKL | VDD = EVDD = 4.0V ~ 5.5V | tCYK/2-13 | | ns |
| | | VDD = EVDD = 3.5V ~ 5.5V | tCYK/2-15 | | |
| Rise time | tKR | VDD = EVDD = 4.0V ~ 5.5V | | 13 | ns |
| | | VDD = EVDD = 3.5V ~ 5.5V | | 15 | |
| Fall time | tKF | VDD = EVDD = 4.0V ~ 5.5V | | 13 | ns |
| | | VDD = EVDD = 3.5V ~ 5.5V | | 15 | |

CLKOUT output timing



2.7.2 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade,
VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|----------------------|-------|------|------|------|
| RESET input low level width | tWRSL | analog filter | 250 | | | ns |
| NMI input high level width | tWNIH | analog filter | 250 | | | ns |
| NMI input low level width | tWNIL | analog filter | 250 | | | ns |
| INTPn ^{Note1} input high level width | tWITH | analog filter ,n=0-8 | 250 | | | ns |
| | | digital filter ,n=3 | Note2 | | | ns |
| INTPn ^{Note1} input low level width | tWITL | analog filter ,n=0-8 | 250 | | | ns |
| | | digital filter ,n=3 | Note2 | | | ns |

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). DRST is same spec (P05/INTP2/DRST)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. RESET, NMI, INTPn, ADTRG and DRST have analog noise filter. The typical filter time is typ=60ns.

2.7.3 Key Return Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade,
VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------|--------|----------------------|------|------|------|------|
| KRn input high level width | tWKRH | analog filter ,n=0-7 | 250 | | | ns |
| KRn input low level width | tWKRL | analog filter ,n=0-7 | 250 | | | ns |

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Timer Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade,
VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------|--------|---|------|------|------|------|
| Tl input high level width | tTIH | TIAA00-01,10-11,20-21,30-31,40-41 ^{Note1} | 250 | | | ns |
| Tl input low level width | tTIL | TIAA00-01,10-11,20-21,30-31,40-41 ^{Note1} | 250 | | | ns |
| TO output cycle | tTCYK | TIAA00-01,10-11,20-21,30-31, 40-41 ^{Note1} | | | 10 | MHz |

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 CSI Timing

(a) Master mode

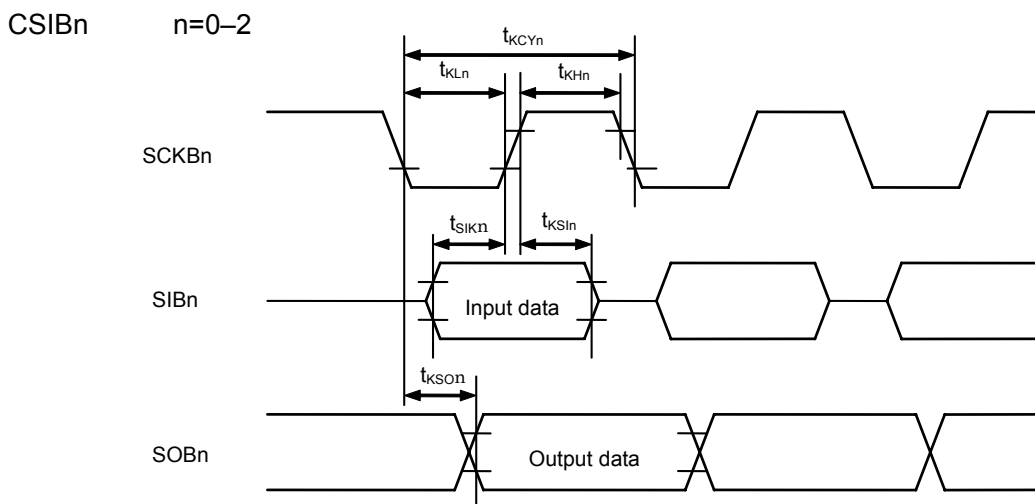
(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|-------------------------------|--------|------------|------------|------|------|
| SCKBn cycle time | tKCY1 | | 125 | | ns |
| SCKBn high level width | tKH1 | | tKCY1/2-15 | | ns |
| SCKBn low level width | tKL1 | | tKCY1/2-15 | | ns |
| SIBn setup time (to SCKBn) | tSIK1 | | 30 | | ns |
| SIBn hold time (from SCKBn) | tKSI1 | | 25 | | ns |
| Delay time from SCKBn to SOBn | tKSO1 | | | 25 | ns |

(b) Slave mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|-------------------------------|--------|------------|------|------|------|
| SCKBn cycle time | tKCY1 | | 200 | | ns |
| SCKBn high level width | tKH1 | | 90 | | ns |
| SCKBn low level width | tKL1 | | 90 | | ns |
| SIBn setup time (to SCKBn) | tSIK1 | | 50 | | ns |
| SIBn hold time (from SCKBn) | tKSI1 | | 50 | | ns |
| Delay time from SCKBn to SOBn | tKSO1 | | | 50 | ns |



2.7.6 UART Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------|--------|------------|------|------|------|------|
| Transfer rate | | | | | 1.5 | Mbps |
| ASCK0 frequency | | | | | 10 | MHz |

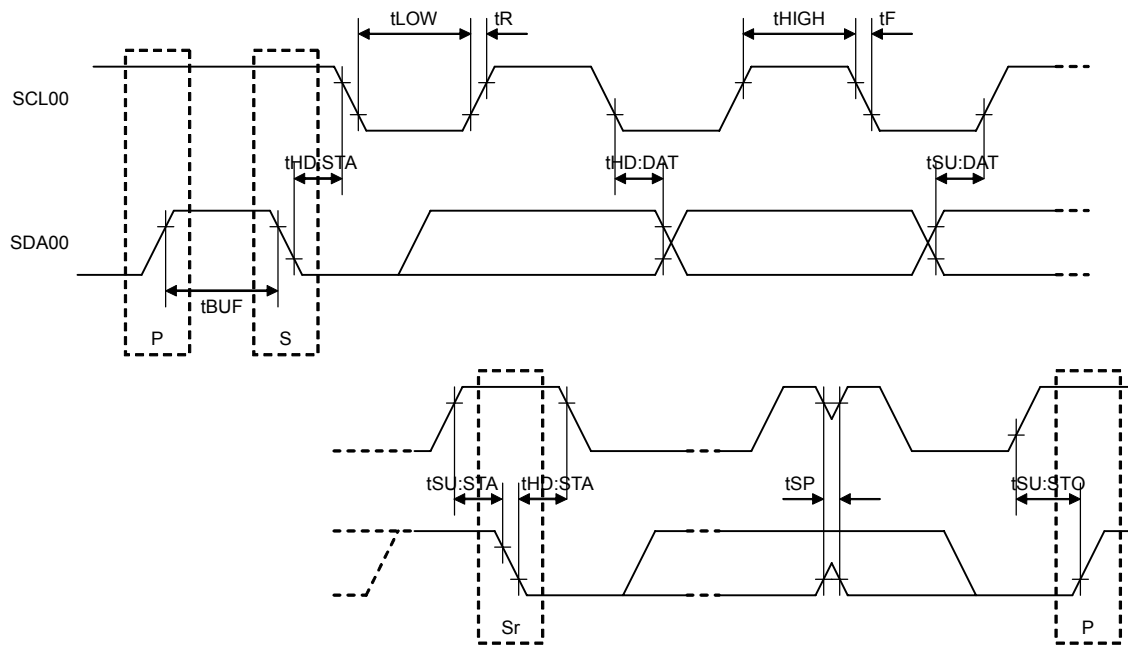
2.7.7 IIC Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade,
VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | | Symbol | Normal mode | | High-speed mode | | Unit |
|---|------------------------|---------|--------------------|------|----------------------|----------------------|------|
| | | | min. | max. | min. | max. | |
| SCL00 clock frequency | | fCLK | 0 | 100 | 0 | 400 | kHz |
| Bus-free time (between stop/start conditions) | | tBUF | 4.7 | | 1.3 | | μs |
| Hold time ^{Note1} | | tHD:STA | 4.0 | | 0.6 | | μs |
| SCL00 clock low-level width | | tLOW | 4.7 | | 1.3 | | μs |
| SCL00 clock high-level width | | tHIGH | 4.0 | | 0.6 | | μs |
| Setup time for start/restart conditions | | tSU:STA | 4.7 | | 0.6 | | μs |
| Data hold time | CBUS compatible master | tHD:DAT | 5.0 | | | | μs |
| | IIC mode | | 0 ^{Note2} | | 0 ^{Note2} | 0.9 ^{Note3} | μs |
| Data setup time | | tSU:DAT | 250 | | 100 ^{Note4} | | ns |
| SDA00 and SCL00 signal rise time | | tR | | 1000 | 20+0.1Cb | 300 | ns |
| SDA00 and SCL00 signal fall time | | tF | | 300 | 20+0.1Cb | 300 | ns |
| Stop condition setup time | | tSU:STO | 4.0 | | 0.6 | | μs |
| Pulse width with spike suppressed by input filter | | tSP | | | 0 | 50 | ns |
| Capacitance load of each bus line | | Cb | | 400 | | 400 | pF |

- Notes:**
- At the start condition, the first clock pulse is generated after the hold time
 - The system requires a minimum of 300ns hold time Internally for the SDA signal (at VIH-min. of SCL00 signal)
In order to occupy the undefined area at the falling edge of SCL00.
 - If the system does not extend the SCL00 signal low hold time (tLOW), only the maximum data hold time (tHD:DAT) needs to be satisfied.
 - The high-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the high-speed-mode IIC bus so that It meets the following conditions.
- If the system does not extend the SCL00 signal's low state hold time:
SU:DAT?250ns
- If the system extends the SCL00 signal's low state hold time:
Transmit the following data bit to the SDA00 line prior to releasing the SCL00 line
(tRmax.+tSU:DAT=1000+250=1250ns: Normal mode IIC bus specification).
 - Cb: Total capacitance of one bus line (unit: pF)

IIC bus interface timing

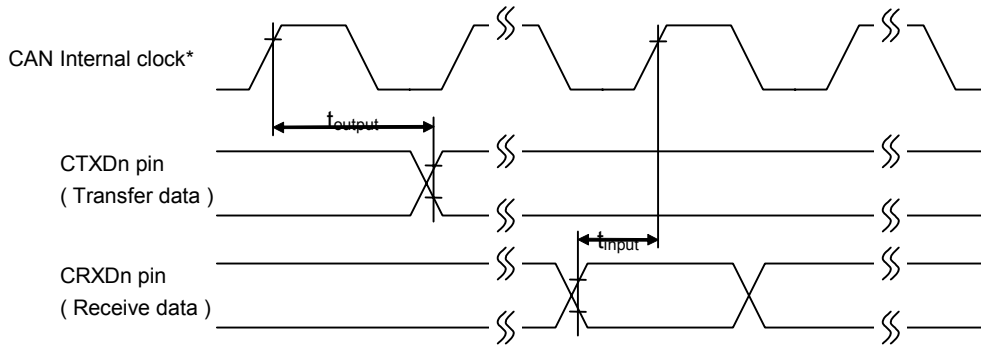


Remark: P: Stop condition
 S: Start condition
 Sr: Restart condition

2.7.8 CAN Timing

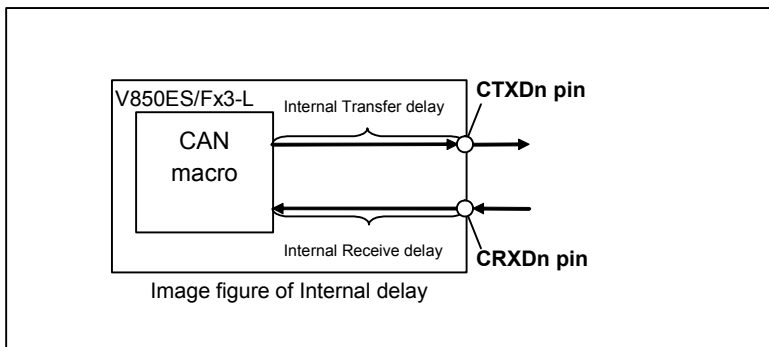
(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------|--------|------------|------|------|------|------|
| Transfer rate | | | | | 1 | Mbps |
| Internal delay time | | | | | 100 | ns |



Internal delay time (t_{NODE})= Internal Transfer Delay(t_{output}) + Internal Receive Delay(t_{input})

*) CAN Internal clock (f_{CAN}) :CAN baud rate clock



2.8 A/D Converter

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 4.0 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | | Unit |
|--|--------|---------------------------|------|-------|----------|-------|------|
| | | | | | (A),(A1) | (A2) | |
| Resolution | | | | | 10 | | bit |
| Overall error ^{Note1} | | 4.0V ≤ AVREF0 < 5.5V | | ±0.15 | ±0.3 | ±0.35 | %FSR |
| Conversion time | tCONV | | 3.10 | | 16 | | µs |
| Stabilization time | tSTA | After ADA0PS bit = 0 -> 1 | 2 | | | | µs |
| Recovery time for power down mode | tDPU | | 1 | | | | µs |
| Zero-scale error ^{Note1} | ZSE | | | | ±0.3 | ±0.35 | %FSR |
| Full-scale error ^{Note1} | FSE | | | | ±0.3 | ±0.35 | %FSR |
| Integral non-linearity error ^{Note2} | INL | | | | ±2.5 | | LSB |
| Differential non-linearity error ^{Note2} | DNL | | | | ±1.5 | | LSB |
| Analog input voltage | VIAN | | AVSS | | AVREF0 | | V |
| Analog input equivalent circuit capacitance ^{Note3,4} | CINA | | | | 6.19 | | pF |
| Analog input equivalent circuit resistance ^{Note3} | RINA | | | | 2.55 | | kΩ |
| AVREF0 current | IAREF0 | A/D operating | | 4 | 7 | | mA |
| | | A/D operation stop | | 1 | 10 | | µA |
| Conversion result when using Diagnostic function | | AVREF0 conversion | 3FC | | 3FF | | HEX |
| | | AVSS conversion | 000 | | 003 | | HEX |

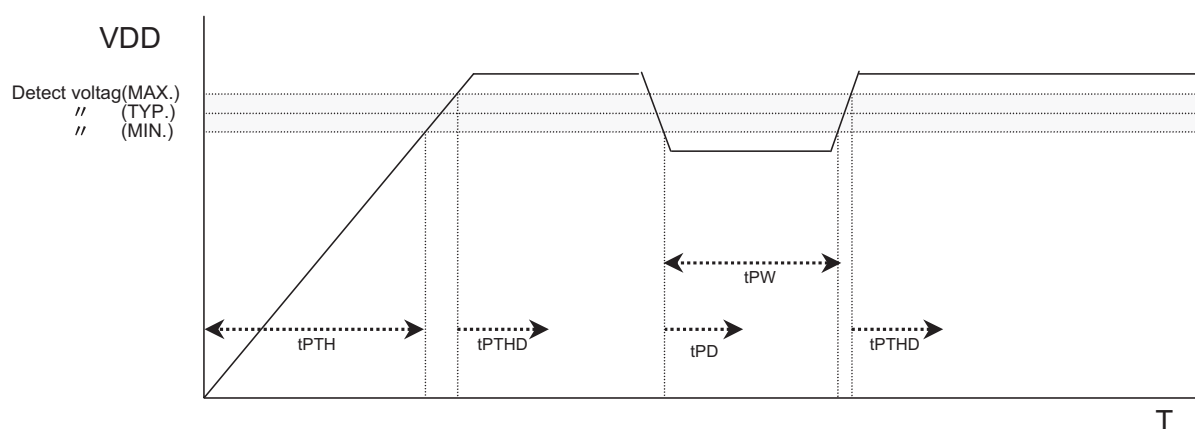
- Notes:**
1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.
 2. Excluding quantization error (±1/2 LSB)
 3. Reference value. Not tested in production.
 4. Does not include input/output capacitance CIO

2.9 POC

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------------|--------|---|-------|------|------|------|
| Detect voltage | VPOC0 | | 3.3 | 3.5 | 3.7 | V |
| Supply voltage rise time | tPTH | From VDD=0V to VDD=3.3V | 0.002 | | | ms |
| Response time1 ^{Note1} | tPTHd | In case of power on. After VDD reaches 3.7V. | | | 2.0 | ms |
| Response time2 ^{Note2} | tPD | In case of power off. After VDD drop 3.3V. | | 0.2 | 1.0 | ms |
| VDD minimum width | tPW | | 0.2 | | | ms |

- Notes:** 1. From detect voltage to release reset signal
 2. From detect voltage to occurrence of reset signal



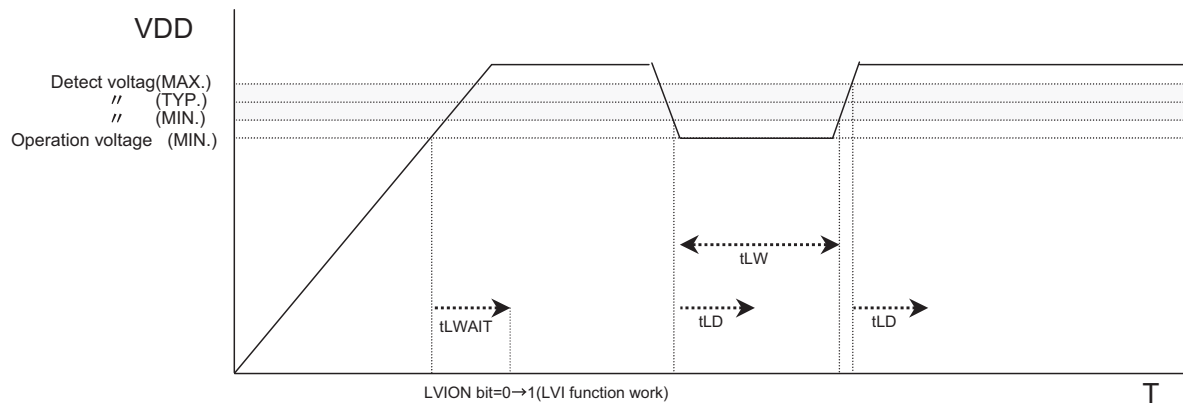
Note: POC is available only in M2 devices. Refer to 'Ordering information' in the V850ES/Fx3-L User'sManual.

2.10 LVI

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|--------|---|------|------|------|------|
| Detect voltage | VLVI0 | | 3.8 | 4.0 | 4.2 | V |
| | VLVI1 | | 3.5 | 3.7 | 3.9 | V |
| Response time ^{Note1} | tLD | After VDD reaches VLVI0/1(max). After VDD drop VLVI0/1(min). | | 0.2 | 2.0 | ms |
| VDD minimum width | tLW | | 0.2 | | | ms |
| Reference voltage stabilization wait time ^{Note2} | tLWAIT | After VDD reaches 3.3V. After LVION bit (LVIM.bit7) = 0->1 | | 0.1 | 0.2 | ms |

- Notes:** 1. From detect voltage to occurrence interrupt/reset signal
 2. If POC functionality is available, the wait time is not needed.

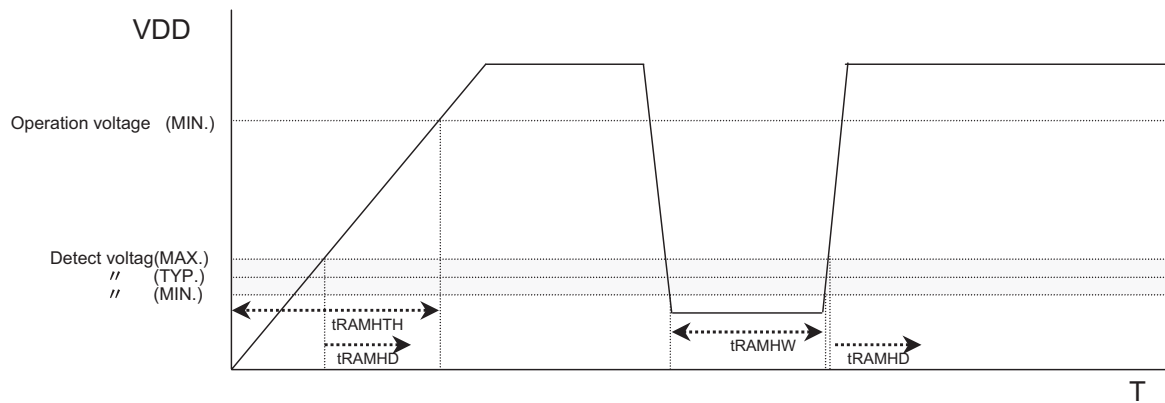


2.11 RAM Retention Flag

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------|---------|-------------------------|-------|------|------|------|
| Detect voltage | VRAMH | | 1.9 | 2.0 | 2.1 | V |
| Supply voltage rise time | tRAMHTH | From VDD=0V to VDD=3.3V | 0.002 | | 1800 | ms |
| Response time ^{Note1} | tRAMHD | After VDD reaches 2.1V. | | 0.2 | 2.0 | ms |
| VDD minimum width | tRAMHW | | 0.2 | | | ms |

- Notes:** 1. From detect voltage to set RAMFbit (RAMS.bit0)

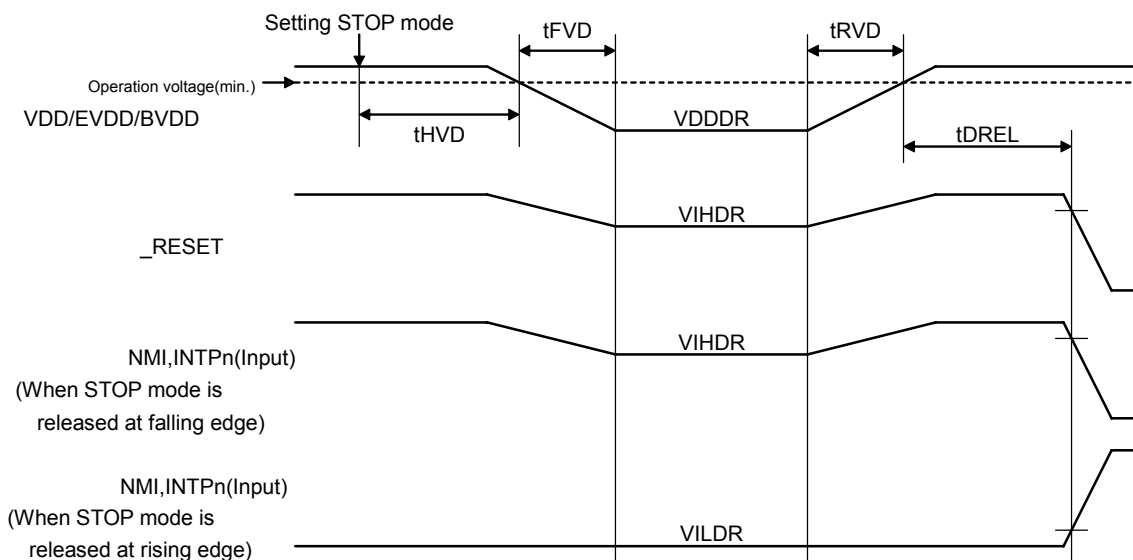


2.12 Data Retention Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V) (

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|--|-----------|------|-----------|------|
| Data retention power supply voltage | VDDDR | STOP mode (All function is stopped) | 1.9 | | 5.5 | V |
| Data retention power supply current | IDDDR | VDDDR=2.0V(All function is stopped) | | 6.5 | 70 | μA |
| Supply voltage rise time | tRVD | | 1 | | | μs |
| Supply voltage fall time | tFVD | | 1 | | | μs |
| Supply voltage hold time | tHVD | After STOP mode | 0 | | | ms |
| STOP release signal input time | tDREL | After VDD reaches operating voltage range MIN. 3.3V | 0 | | | ms |
| Data retention high-level input voltage | VIHDR | All input port | 0.9·VDDDR | | VDDDR | V |
| Data retention low-level input voltage | VILDR | All input port | 0 | | 0.1·VDDDR | V |

Remark: When STOP mode is entered/released operation voltage range must be controlled.



2.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | | | Unit |
|--------------------------|--------|------------|----------|------|----------|------|------|-------|
| | | | | | (A) | (A1) | (A2) | |
| Operation frequency | fCPU | | 4 | | 20 | | | MHz |
| Supply voltage | VDD | | 3.3 | | 5.5 | | | V |
| Number of rewrites | CWRT | Code Flash | | | 1000 | | | count |
| High level input voltage | VIH | FLMD0 | 0.8·EVDD | | EVDD | | | V |
| Low level input voltage | VIL | FLMD0 | EVSS | | 0.2·EVDD | | | V |
| Programming temperature | tPRG | | -40 | | +85 | +110 | +125 | °C |
| Data retention | | Code Flash | 15 | | | | | year |

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

Example: P: Program(write) E: Erase

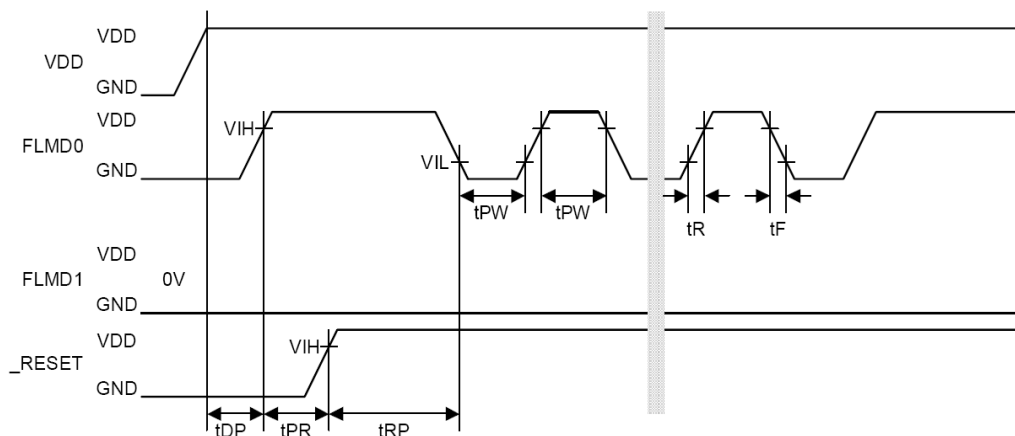
Product is shipped → P → E → P → E → P : Rewrite count: 3

Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

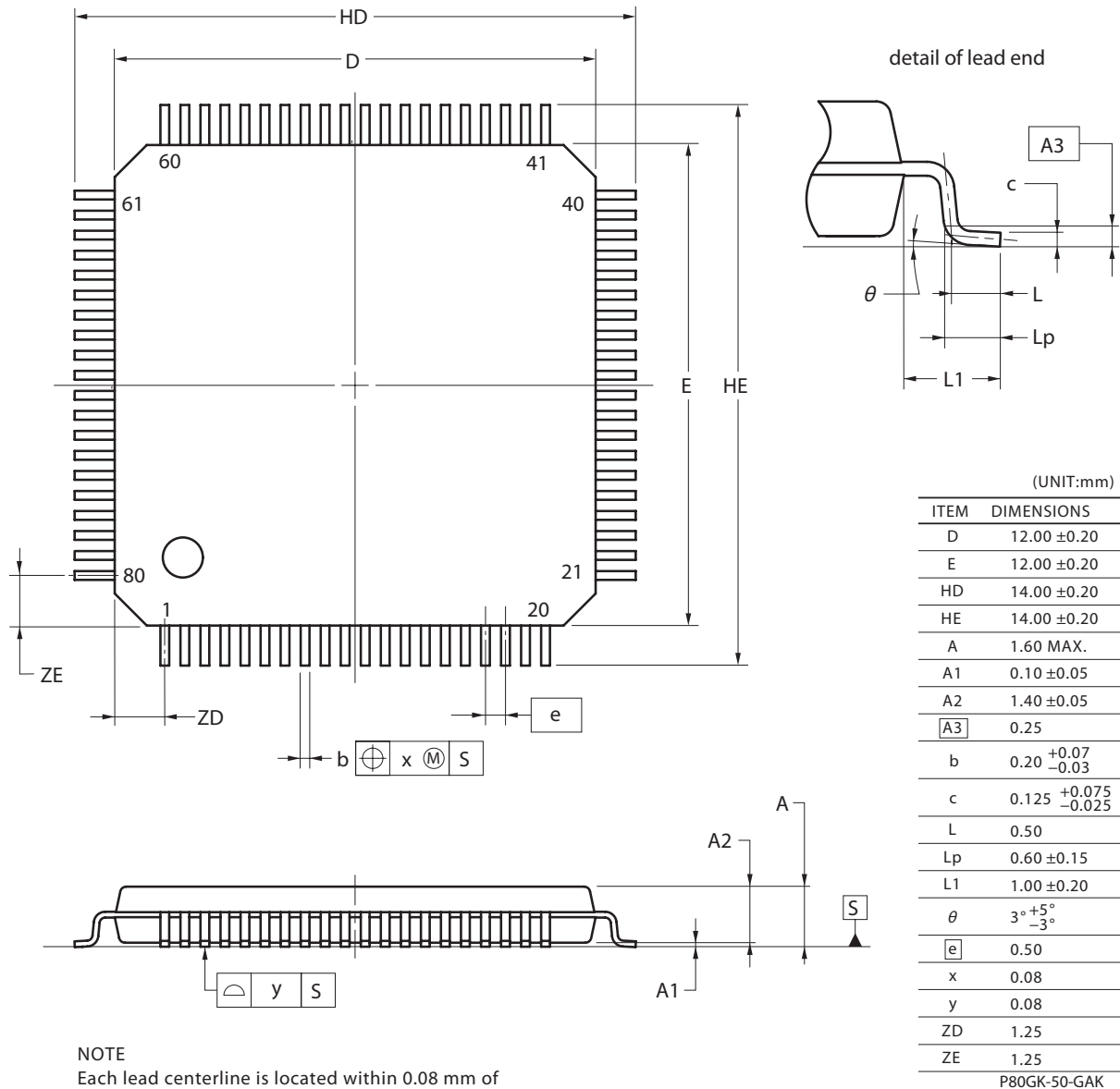
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|------------|------|------|------|------|
| FLMD0 setup time (from VDD) | tDP | | 1 | | | ms |
| RESET release (from FLMD0) | tPR | | 2 | | | ms |
| FLMD0 pulse input start (from raise edge of _RESET) | tRP | | 800 | | | µs |
| FLMD0 high level width / low level width | tPW | | 10 | | 100 | µs |
| FLMD0 raise time | tR | | | | 50 | ns |
| FLMD0 fall time | tF | | | | 50 | ns |



3. Package

3.1 Package Dimension

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)

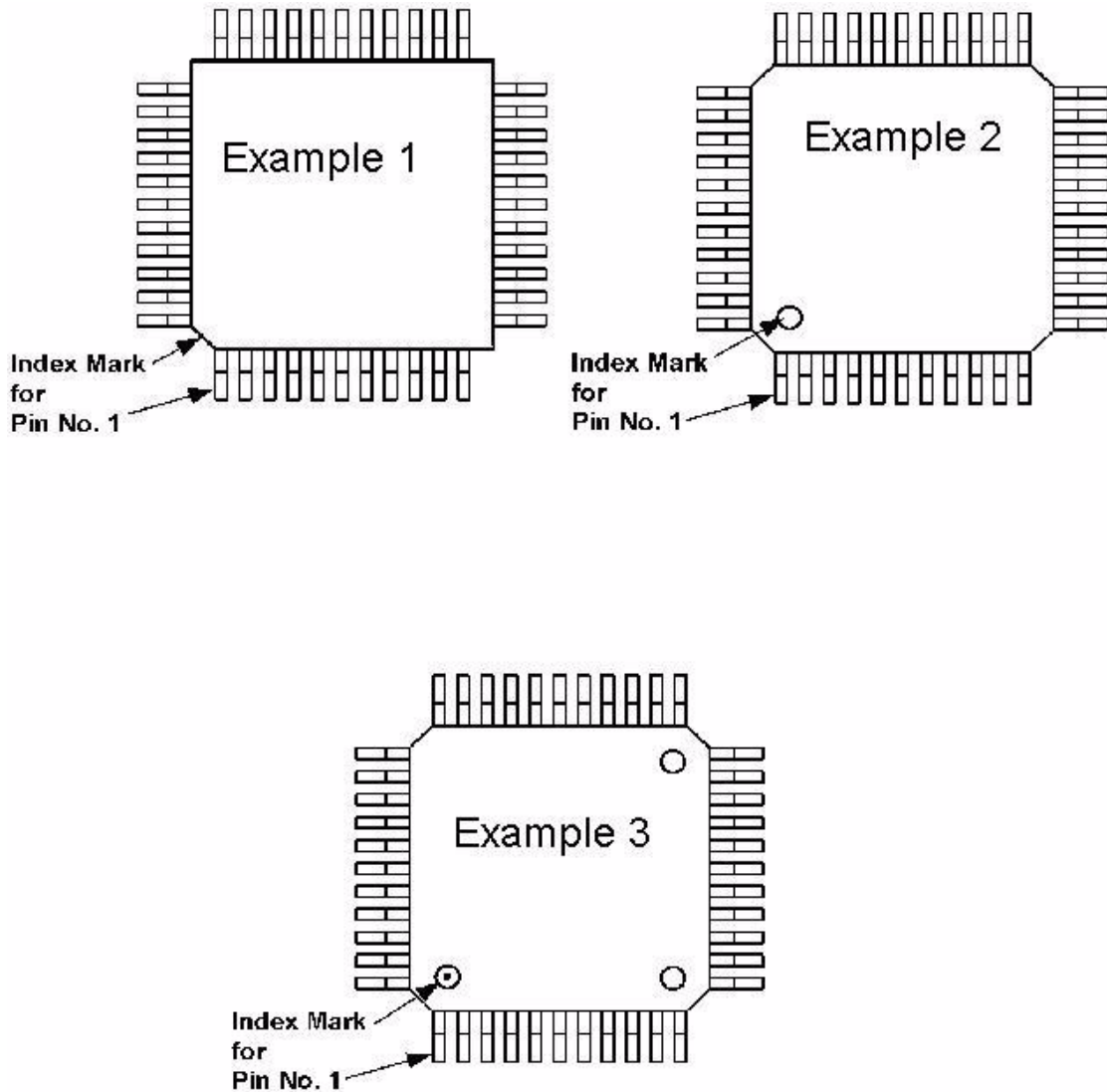


NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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3.2 Product Marking

3.2.1 Marking of pin 1 at a QFP (Quad Flat Package)



Example 1: The index mark for pin 1 is the beveled edge of the package

Example 2: The index mark for pin 1 is a round notch at one of the 4 edges. In this case, the shape of all edges is identical (usually beveled).

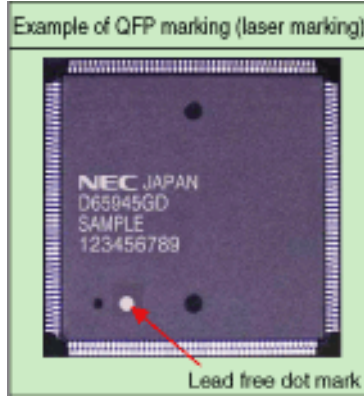
Example 3: For production reasons, two or more similar notches may be located at the top of the package. In such a case the index marker for pin 1 is a round notch with an additional mark in it.

Note: RoHS compliant devices have an additional dot at the top side. Do not mix it up with the marking for pin 1. For details see 3.2.2 "Identification of Lead-Free Products" on page 34.

3.2.2 Identification of Lead-Free Products

Lead-Free products are marked with a dot "•". The marking methods are the paint or the laser (It doesn't sink in). The shape of lead-free marks is a circle.

Example:



4. Change History

| Version | Chapter | Comment |
|---------|---------|-----------------|
| V1.0 | | Initial release |

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