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November 3, 2004 FN9193.0

Triple Output, Low-Noise LDO Regulator with Integrated Reset Circuit

The ISL6416 is an ultra low noise triple output LDO regulator with microprocessor reset circuit and is optimized for powering wireless chip sets. The IC accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.8V (LDO1), 2.8V (LDO2), and another ultra-clean 2.8V (LDO3). On chip logic provides sequencing between LDO1 and LDO2 for the BBP/MAC and the I/O supply voltage outputs. LDO3 features ultra low noise that does not exceed 30µV_{RMS} (typical) to aid VCO stability. High integration makes the ISL6416 an ideal choice to power many of today's small form factor industry standard wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

The ISL6416 uses an internal PMOS transistor as the pass device. The ISL6416 also integrates a reset function, which eliminates the need for the additional reset IC required in WLAN applications. The IC asserts a $\overline{\text{RESET}}$ signal whenever the VIN supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after Vin has risen above the reset threshold. FAULT indicates the loss of regulation on LDO1.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6416IA	-40 to +85	16 Ld QSOP	M16.15A
ISL6416IAZ (Note 1)	-40 to +85	16 Ld QSOP (Pb-free)	M16.15A

NOTES:

1. Tape and Reel available. Add "-T" suffix for Tape and Reel Packing Option.
2. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Features

- Three LDOs and a RESET circuit
- High Output Current
  - LDO1, 1.8V 330mA
  - LDO2, 2.8V 225mA
  - LDO3, 2.8V 125mA
- Low Output Voltage Noise
  - <30µV_{RMS} (typical) for LDO3 (VCO Supply)
- Stable with Small Ceramic Output Capacitors
- Extensive Protection and Monitoring Features
  - Overcurrent protection
  - Short circuit protection
  - Thermal shutdown
  - FAULT indicator
- Logic-Controlled Shutdown Pin
- Integrated Microprocessor Reset Circuit
  - Programmable Reset Delay
- Proven Reference Design for a Total WLAN System Solution
- Pb-Free Available (RoHS Compliant)

Applications

- WLAN Cards
  - PCMCIA, Cardbus32, MiniPCI Cards
  - Compact Flash Cards
- Hand-Held Instruments

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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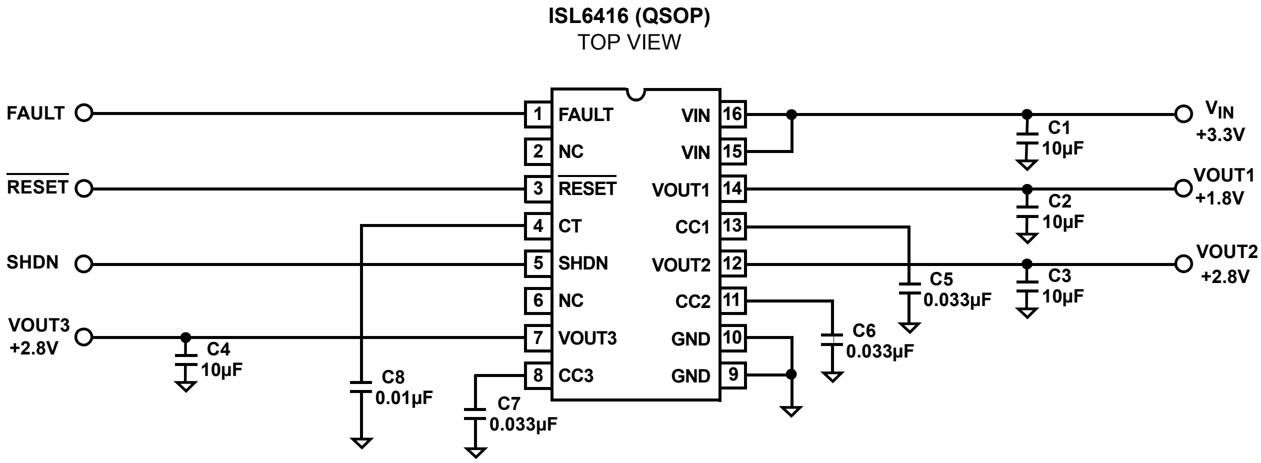
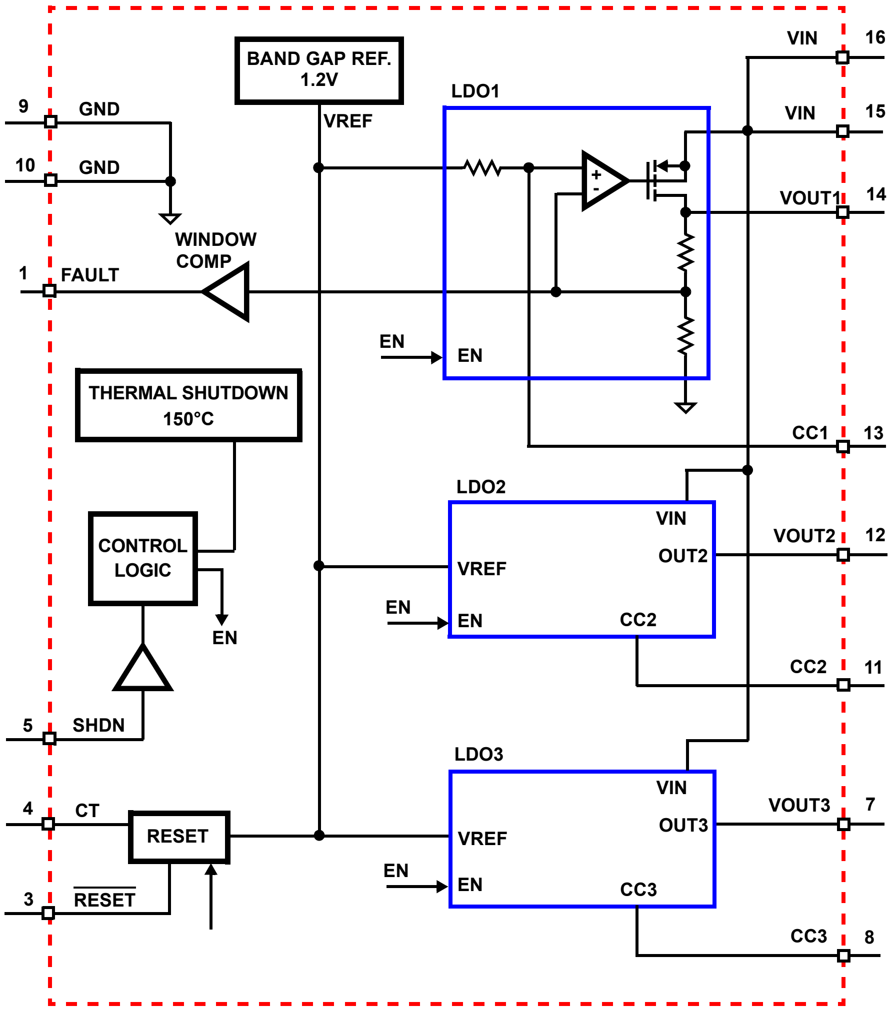
Pinout and Typical Application Schematic



Typical Bill Of Materials

REFERENCE DESIGNATOR	VALUE	PACKAGE	MANUFACTURER	MANUFACTURER'S PART NUMBER
C1, C2, C3, C4	10µF, X7R	1206	TDK	C3216X7R1A106M
C5, C6, C7	0.033µF, X7R	0603	TDK/ANY	C1608X7R1A333K
C8	0.01µF, X7R	0603	TDK/ANY	C1608X7R1A103K
U1	ISL6416IA	QSOP16	Intersil	ISL6416IA

Functional Block Diagram



Absolute Maximum Ratings

V_{IN}, SHDN to GND 7.0V
RESET, CC, FAULT to GND . . . . -0.3V to 7.0V
Output Current (Continuous)
LDO1 . . . . 330mA
LDO2 . . . . 225mA
LDO3 . . . . 125mA
ESD Classification . . . . Class 1

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
QSOP Package (Note 3) 105
Maximum Junction Temperature (Plastic Package) . -55°C to 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
Operating Temperature Range . . . . -40°C to 85°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications

V_{IN} = +3.3V, Compensation Capacitor = 33nF, T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL SPECIFICATIONS					
V_{IN} Voltage Range		3.0	3.3	3.6	V
Operating Supply Current	IOUT = 0mA	-	830	-	µA
Shutdown Supply Current	SHDN = GND	-	5	10	µA
SHDN Input Threshold	VIH, VIN = 3V to 3.6V	2.0	-	-	V
	VIL, VIN = 3V to 3.6V	-	-	0.4	V
Thermal Shutdown Temperature (Note 6)		145	150	160	°C
Thermal Shutdown Hysteresis (Note 6)		-	20	-	°C
Start-up Time (Note 6)	C_{OUT} = 10µF, V_{OUT} = 90% of final value	-	120	-	µs
Input Undervoltage Lockout (Note 6)	Rising 75mV Hysteresis	2.4	2.45	2.6	V
LDO1 SPECIFICATIONS					
Output Voltage (V_{OUT1})		-	1.8	-	V
Output Voltage Initial Accuracy	I_{OUT} = 10mA, T_A = -40°C to 85°C	-2.0	-	2.0	%
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 330mA	-1.5	-	1.5	%
Maximum Output Current (I_{OUT1})	VIN = 3.3V	330	-	-	mA
Output Current Limit		500	-	-	mA
Output Voltage Noise (Note 6)	10Hz < f < 100kHz, C_{OUT} = 4.7µF, I_{OUT} = 50mA	-	115	-	μV_{RMS}
LDO2 SPECIFICATIONS					
Output Voltage (V_{OUT2})		-	2.8	-	V
Output Voltage Accuracy	I_{OUT} = 10mA, T_A = -40°C to 85°C	-2.0	-	2.0	%
Maximum Output Current (I_{OUT2})	VIN = 3.3V	225	-	-	mA
Output Current Limit		330	-	-	mA
Dropout Voltage (Note 4)	I_{OUT} = 225mA	-	75	200	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 225mA	-1.0	0.2	1.0	%

Electrical Specifications

V_{IN} = +3.3V, Compensation Capacitor = 33nF, T_A = 25°C, unless otherwise noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Noise (Note 6)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	65	-	μV_{RMS}
	C_{OUT} = 10µF	-	60	-	μV_{RMS}
LDO3 SPECIFICATIONS					
Output Voltage (V_{OUT3})		-	2.8	-	V
Output Voltage Accuracy	I_{OUT} = 10mA, T_A = -40°C to 85°C	-2.0	-	2.0	%
Maximum Output Current (I_{OUT3})	VIN = 3.3V	125	-	-	mA
Output Current Limit		300	-	-	mA
Dropout Voltage (Note 4)	I_{OUT} = 125mA	-	65	200	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 125mA	-1.0	0.2	1.0	%
Output Voltage Noise (Note 6)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	30	-	μV_{RMS}
	C_{OUT} = 10µF	-	20	-	μV_{RMS}
RESET BLOCK SPECIFICATIONS					
Reset Threshold		2.564	2.630	2.66	V
Reset Threshold Hysteresis (Note 5)		6.3	-	-	mV
V_{IN} to Reset Delay (Note 5)	VCC = V_{TH} to V_{TH} - 100mV	-	20	-	µs
$\overline{RESET}$ Active Timeout Period (Note 5)	CT = 0.01µF	50	-	-	ms
FAULT					
Rising Threshold	% of V_{OUT}	+5.5	+8.0	+10.5	%
Falling Threshold	% of V_{OUT}	-10.5	-8.0	-5.5	%

4. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 50mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V.
5. The $\overline{RESET}$ time is linear with CT at a slope of ~5ms/nF. Thus, at 10nF (0.01µF) the $\overline{RESET}$ time is 50ms.
6. Guaranteed by design, not production tested.

Typical Performance Curves

The test conditions for the Typical Operating Performance are: V_{IN} = 3.3V, T_A = 25°C, Unless Otherwise Noted

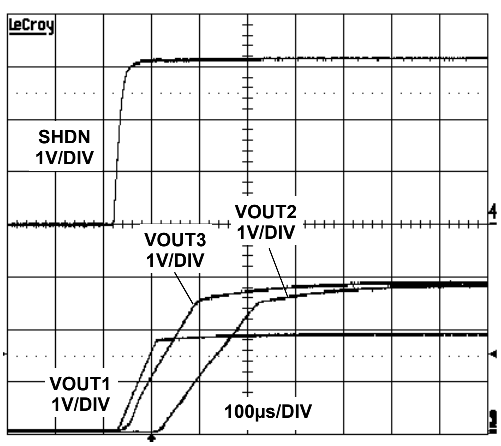


FIGURE 1. START-UP SEQUENCE

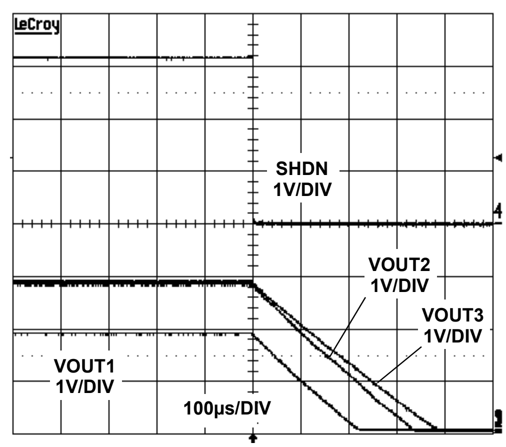


FIGURE 2. SHUTDOWN SEQUENCE

Typical Performance Curves

The test conditions for the Typical Operating Performance are: V_{IN} = 3.3V, T_A = 25°C, Unless Otherwise Noted **(Continued)**

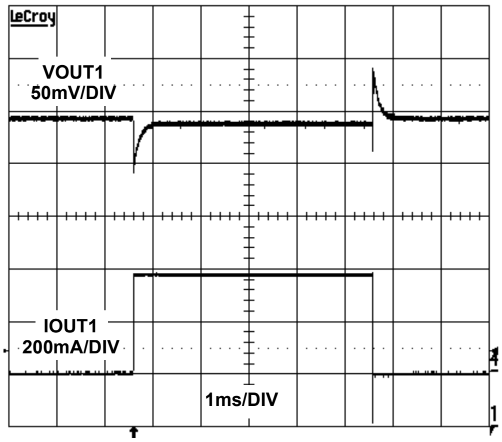


FIGURE 3. LDO1 LOAD TRANSIENT RESPONSE (10mA to 380mA)

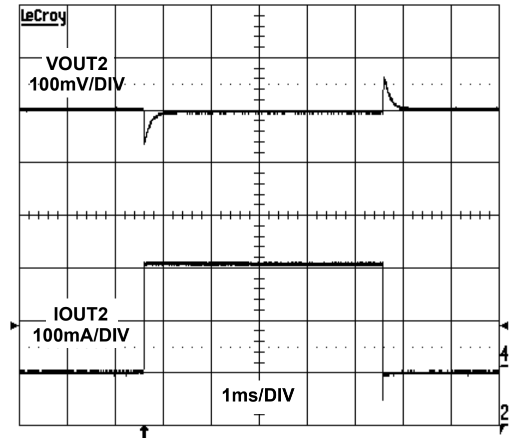


FIGURE 4. LDO2 LOAD TRANSIENT RESPONSE (10mA to 200mA)

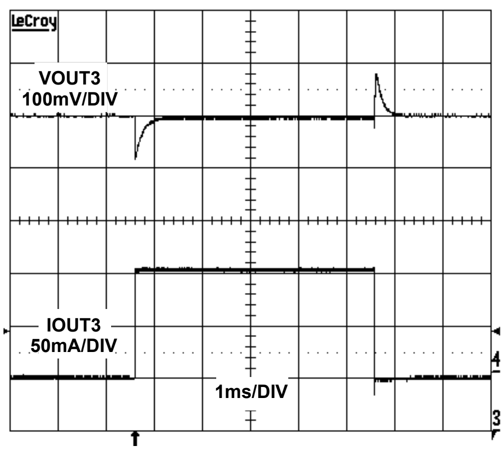


FIGURE 5. LDO3 LOAD TRANSIENT RESPONSE (10mA to 100mA)

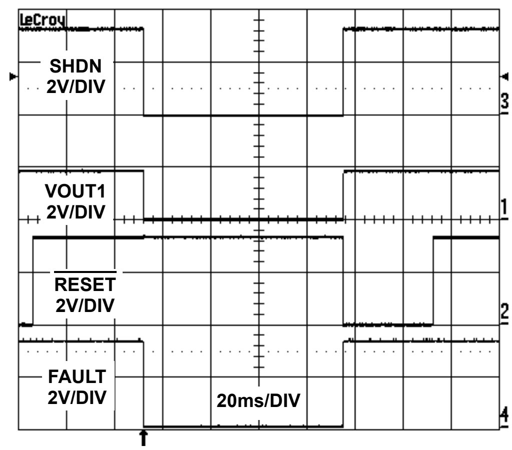


FIGURE 6. SHUTDOWN FAULT AND RESET OPERATION

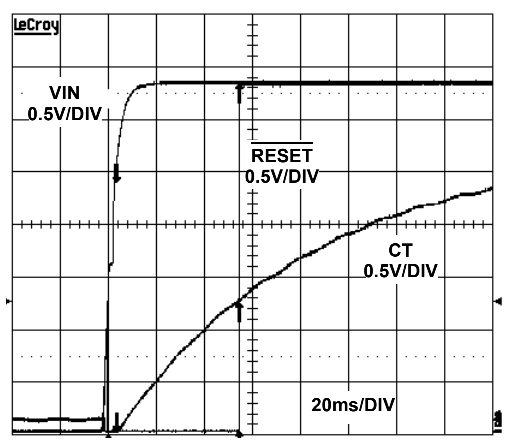


FIGURE 7. RESET DELAY DURING START-UP (CT = 0.01µF)

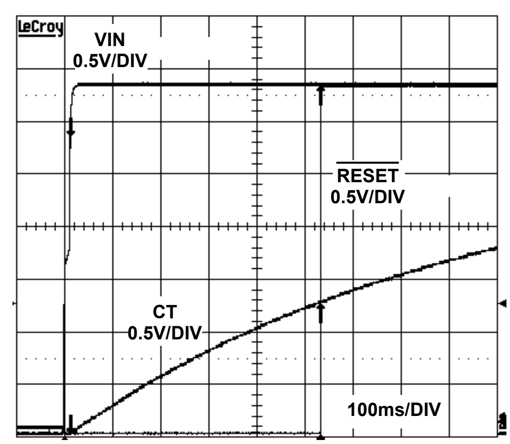


FIGURE 8. RESET DELAY DURING START-UP (CT = 0.1µF)

Typical Performance Curves

The test conditions for the Typical Operating Performance are: V_{IN} = 3.3V, T_A = 25°C, Unless Otherwise Noted **(Continued)**

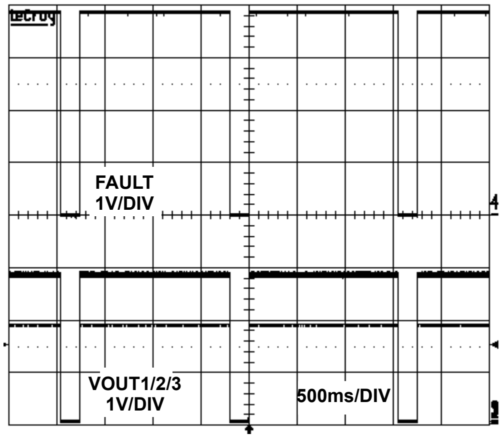


FIGURE 9. THERMAL SHUTDOWN OPERATION

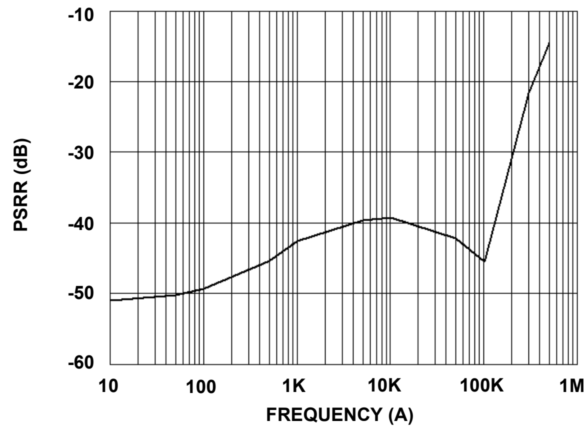


FIGURE 10. LDO1 POWER SUPPLY REJECTION (IOUT1 = 100mA, COUT = 10µF CERAMIC)

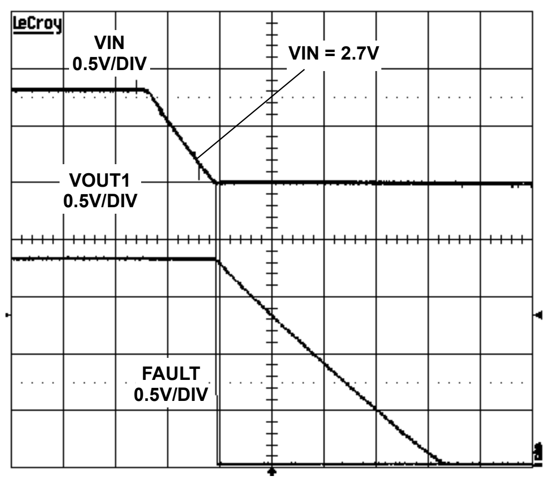


FIGURE 11. VOUT1 REGULATION DOWN TO VIN = 2.7V. FAULT MONITORS VOUT1 ONLY

Pin Descriptions

VOUT1 - This pin is the output for LDO1. Bypass with a minimum of 2.2µF, low ESR ceramic capacitor to GND for stable operation.

V_{IN} - Supply input pins. Connect to input power source. Bypass with a minimum 2.2µF capacitor to GND. Both V_{IN} pins must be tied together on the PC board, close to the IC.

GND - Ground for LDO1, LDO2, and LDO3.

CC1 - Compensation Capacitor for LDO1. Connect a 0.033µF capacitor from CC1 to GND.

SHDN - Shutdown input for all LDOs. This pin is pulled up internally. Drive this pin LOW to turn off all LDOs.

VOUT2 - This pin is the output for LDO2. Bypass with a minimum of 2.2µF, low ESR capacitor to GND for stable operation.

CT - Timing pin for the $\overline{\text{RESET}}$ circuit pulse width. A capacitor connected from this pin to GND will set a delay the $\overline{\text{RESET}}$ delay. Leaving this pin open will make the $\overline{\text{RESET}}$ delay approximately zero.

CC2 - Compensation capacitor for LDO2. Connect a 0.033µF capacitor from CC2 to GND.

VOUT3 - This pin is output for LDO3. Bypass with a minimum of 2.2µF, low ESR capacitor to GND3 for stable operation.

CC3 - Compensation capacitor for LDO3. Connect a 0.033µF capacitor from CC3 to GND3.

FAULT - This is the power good indicator for LDO1. When the 1.8V output is out of regulation this pin goes LOW. This pin also goes LOW during thermal shutdown or an overcurrent event on LDO1. Leave floating if not used.

$\overline{\text{RESET}}$ - This pin is the active-LOW output of the push-pull output stage of the integrated reset supervisory circuit. The reset circuit monitors V_{IN} and asserts a $\overline{\text{RESET}}$ output at this pin, if V_{IN} falls below the reset threshold. The $\overline{\text{RESET}}$ output remains LOW, while the V_{IN} pin voltage is below the reset threshold, and for a time set by the CT capacitor, after V_{IN} rises above the reset threshold.

Functional Description

The ISL6416 is a 3-in-1 multi-output, low dropout, regulator designed for wireless chipset power applications. It supplies three fixed output voltages 1.8V, 2.8V and 2.8V. Each LDO consists of a 1.2V reference, error amplifier, MOSFET driver, P-Channel pass transistor, dual-mode comparator and internal feedback voltage divider.

The 1.2V band gap reference is connected to the error amplifier's non-inverting input. The error amplifier compares this reference to the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-Channel pass transistor. If the feedback voltage is lower then the reference voltage, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the pass transistor gate is driven higher, allowing less current to pass to the output. The output voltage is fed back through an internal resistor divider connected to OUT1/2/3 pins.

Additional blocks include an output overcurrent protection, thermal sensor, fault detector, $\overline{\text{RESET}}$ function and shutdown logic.

Internal P-Channel Pass Transistors

The ISL6416 features a typical 0.5Ω $r_{DS(ON)}$ P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL6416 does not suffer from these problems.

Integrated Reset for MAC/ Baseband Processors

The ISL6416 includes a microprocessor supervisory block. This block eliminates the extra reset IC and external components needed in wireless chipset applications. This block performs a single function; it asserts a $\overline{\text{RESET}}$ signal whenever the V_{IN} supply voltage decreases below a preset threshold, keeping it asserted for a programmable time (set by external capacitor CT) after the V_{IN} pin voltage has risen above the reset threshold. The reset threshold for the ISL6416 is 2.63V typical.

The voltage at the CT pin is compared to the 1.2V bandgap voltage. The charging of the CT capacitor behaves like an RC network and the $\overline{\text{RESET}}$ delay can be approximated by:

Td = -R*C*ln(1-1.2V/VIN)

Where C is the capacitor at CT, and R is 11.1MΩ for VIN = 3.3V. With no capacitor on the CT pin the $\overline{\text{RESET}}$ delay will be close to zero. Figure 12 shows the $\overline{\text{RESET}}$ delay vs CT capacitance.

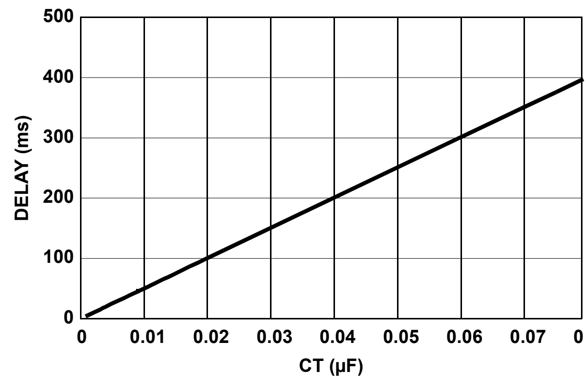


FIGURE 12. RESET DELAY vs CT CAPACITANCE

Output Voltages

The ISL6416 provides fixed output voltages for use in Wireless Chipset applications. Internal trimmed resistor networks set the typical output voltages as shown here:

V_{OUT1} = 1.8V; V_{OUT2} = 2.8V; V_{OUT3} = 2.8V.

Shutdown

Pulling the SHDN pin LOW puts the complete chip into shutdown mode, and supply current drops to 5µA typical. This input has an internal pull-up resistor, so that in normal operation the outputs are always enabled; external pull-up resistors are not required.

Current Limit

The ISL6416 monitors and controls the pass transistor's gate voltage to limit the output current. The current limit for LDO1 is 500mA, LDO2 is 330mA and LDO3 is 300mA. The output can be shorted to ground without damaging the part due to the current limit and thermal protection features.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL6416. When the junction temperature (T_J) exceeds +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The pass transistor turns on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection protects the ISL6416 against fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Operating Region and Power Dissipation

The maximum power dissipation of ISL6416 depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated in the device is:

PT = P1 + P2 + P3, where

P1 = Iout1 (Vin – Vout1)

P2 = Iout2 (Vin – Vout2)

P3 = Iout3 (Vin- Vout3)

The maximum power dissipation is:

$P_{max} = (T_{jmax} - T_A)/\theta_{JA}$

Where Tjmax = 150°C, T_A = ambient temperature, and θ_{JA} is the thermal resistance from the junction to the surrounding environment.

Integrator Circuitry

The ISL6416 uses an external 33nF compensation capacitor for minimizing load and line regulation errors and for lowering output noise. When the output voltage shifts due to varying load current or input voltage, the integrator capacitor voltage is raised or lowered to compensate for the systematic offset at the error amplifier. Compensation is limited to ±5% to minimize transient overshoot when the device goes out of dropout, current limit, or thermal shutdown.

FAULT Functionality

TABLE 1.

EVENT	FAULT
Below UVLO threshold	L
VOUT1 = 1.8V ±8% typ VOUT2/3 not in regulation	H
VOUT1 not in regulation VOUT2 and VOUT3 are in regulation	L
Thermal Shutdown	L
Normal Shutdown with SHDN pin	L
Overcurrent only on LDO1	L
Overcurrent only on LDO2/LDO3	H

Applications Information

Capacitor Selection and Regulator Stability

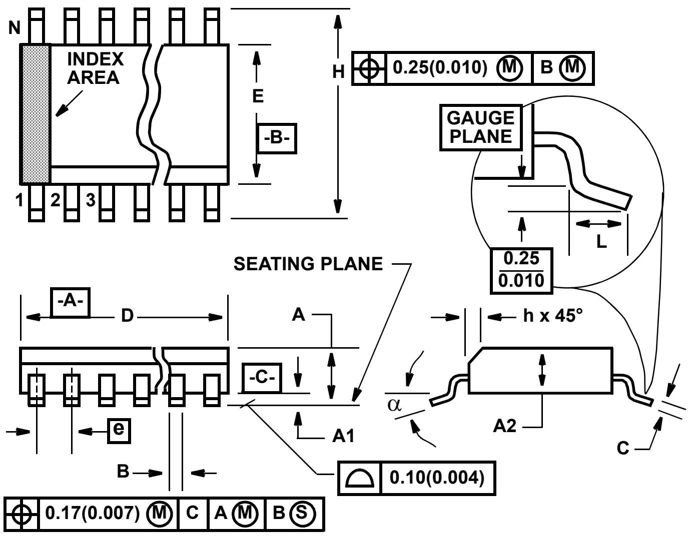
Capacitors are required at the ISL6416's input and output for stable operation over the entire load range and the full temperature range. Use > 2.2µF capacitor at the input of ISL6416. The input capacitor lowers the source impedance of the input supply. Larger capacitor values and lower ESR provides better PSRR and line transient response. The input capacitor must be located as close as possible to the VIN pins of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used as an input capacitor.

The output capacitor must meet the requirements of minimum amount of capacitance and ESR for all three LDO's. The ISL6416 is specifically designed to work with small ceramic output capacitors. The output capacitor's ESR affects stability and output noise. Use an output capacitor with an ESR of 50mΩ or less to insure stability and optimum transient response. For stable operation, a ceramic capacitor, with a minimum value of 3.3µF, is recommended for V_{OUT1} for 300mA output current, and 2.2µF is recommended for V_{OUT2} and V_{OUT3} each at 200mA load current. There is no upper limit to the output capacitor value. A larger capacitor can reduce noise and improve load transient response, stability and PSRR. Higher value of the output capacitor (10µF) is recommended for LDO3 when used to power VCO circuitry in wireless chipsets. The output capacitor should be located very close to Vout pins to minimize impact of PC board inductances and the other end of the capacitor should be returned to a clean analog ground.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. Because the ISL6416 uses a P-channel MOSFET pass transistor, its dropout voltage is a function of $r_{DS(ON)}$ (typically 0.5) multiplied by the load current.

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



M16.15A

16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150" WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.061	0.068	1.55	1.73	-
A1	0.004	0.0098	0.102	0.249	-
A2	0.055	0.061	1.40	1.55	-
B	0.008	0.012	0.20	0.31	9
C	0.0075	0.0098	0.191	0.249	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.81	3.99	4
e	0.025 BSC		0.635 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.89	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 2 6/04

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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